Functional Material Microstructure of Antimony Oxide (Sb_2O_3) Molecular Crystal Gate Dielectrics

Alok Ranjan[1], Kailang Liu[2], Tianyou Zhai[2], Eva Olsson[1]

[1]*Department of Physics, Chalmers University of Technology, Gothenburg, Sweden*

[2]*Huazhong University of Science and Technology, Hubei, China*

Extended Abstract

2D materials based nanoelectronics[1] has drawn significant interest as it has potential to outperform Si technology in many emerging applications. Gate insulator and its interface with the channel material in a transistor are the key factors deciding technological feasibility of a semiconductor channel material considered. Conventional CMOS gate dielectrics (e.g., SiO_2, HfO_2) form a poorer interface with 2D materials rendering and an alternative solution is needed. Compatible van der Waals gate dielectric materials are now instead actively explored which could seamlessly be integrated with 2D layered materials.

Sb_2O_3 is of particular interest as (*i*) the material has a higher dielectric constant ($\kappa = 11.5$) and (*ii*) it can be grown on a wafer scale with a tighter control on the thickness and defect density[2], which are the pre-requisites for a gate dielectric material to be integrated with 2D materials[3]. We present some results from an ongoing work where we are investigating the reliability of Sb_2O_3 dielectrics by combining charge transport measurements at device level, and physical and chemical analysis at nanoscale using transmission electron microscopy (TEM).

A thin film of Sb_2O_3 dielectric is deposited on 4" pre-cleaned $n^{++}Si$ substrates using thermal evaporation deposition. Lithography is used to prepare capacitor test structures and a top electrode is deposited using electron beam evaporation. The capacitor area varies between 50×50 μm^2 and 100×100 μm^2. Electrical measurements are carried using a semiconductor parameter analyser allowing us to probe the defect generation and degradation in a wide current range varying from pA to mA. Measurements are carried out at room temperature and the bias is applied to the top electrode while the Si substrate is grounded.

Prior to electrical measurements, a cross section of the sample is prepared using focused ion beam. TEM analysis is used to confirm that the Sb_2O_3 has a uniform thickness of 7 nm as shown in **Figure 1a**. An additional 2 nm thick SiO_x interfacial layer is also present between the Si substrate and the Sb_2O_3 layer. *I-V* measurements are carried out on capacitors of varying area and the data confirms that the tunnel current scales with device area showing a homogeneous conduction as shown in **Fig. 1b**. Pre-existing atomic defects in Sb_2O_3 show random telegraph noise (not shown here for brevity). Finally, *I-V* breakdown measurements in **Fig. 1c** show that the breakdown field strength is 2-3 MV/cm. Statistical analysis of the breakdown data in **Fig. 1d** shows that it follows a Weibull model[4].

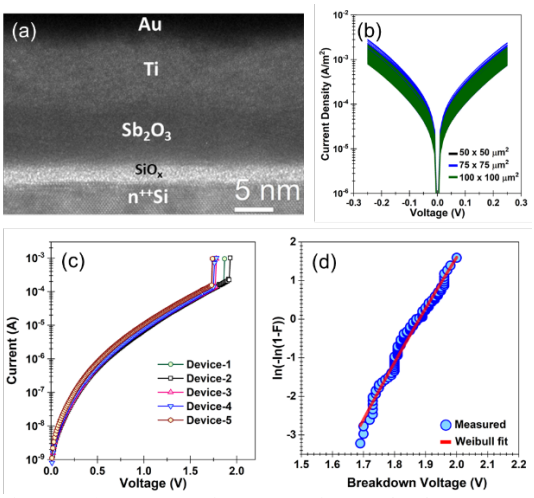

Figure 1: (a) Cross-section TEM micrograph of an as prepared $n^{++}Si/Sb_2O_3/Ti$ capacitor. (b) Plot showing scaling of current with device area. (c) *I-V* breakdown characteristics, and (d) Weibull plot showing the distribution of breakdown voltage. 80 devices are tested for data shown in (d) and area of capacitor is 100×100 μm^2.

Conclusions: Initial reliability analysis of Sb_2O_3 shows that it has excellent thickness control and highly uniform *I-V* characteristics across all the devices measured on 4" wafer. Statistical analysis confirms that the defect generation is random and follows the Weibull model. The reliability can be further improved by suppressing the growth of interfacial SiO_x layer.

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