Curriculum Vitae of Per Stenström

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Education

- Docent (habilitation) in Electrical and Computer Engineering, Lund University, 1993
- PhD in Computer Engineering, Lund University, 1990
- MSc in Electrical Engineering (Civilingenjör in Swedish), Lund University, 1981

Appointments (Academic)

- Professor, Computer Architecture, Chalmers University of Technology, since 1995
- Visiting Professor, Lund University, since 2023
- Guest Professor, Gothenburg University, 2004 – 2006
- Associate Professor, Lund University, 1993 – 1995
- Research Associate, Swedish Institute of Computer Science, 1993 – 1998
- Visiting Scholar, University of Southern California, 1993
- Visiting Scholar, Stanford University, 1991
- Senior Lecturer, Lund University, 1988 – 1993
- Visiting Scholar, Carnegie Mellon University, 1987 – 1988
- Research Assistant, Lund University, 1984 – 1988

Appointments (Industry)

- Co-founder, Board member, InfiniNode Technologies AB, since 2025
- Co-founder, Chief Science Officer, Board member, ZeroPoint Technologies AB, since 2015
- Co-founder, CEO/CTO, Board member, Nema Labs AB, 2007 – 2012
- Consultant, Sun Microsystems, 2003 – 2006
- Senior Staff Engineer, Sun Microsystems, 2002 – 2003
- Board member, Virtutech AB, 1998 – 2002
- Systems Engineer, ABB, 1983 – 1984
- Systems Engineer, Kockumation, 1981 – 1983

Leadership Roles

- Division head of Computer Engineering, Chalmers, 2015 – 2023
- Deputy Dean, IT Faculty, Gothenburg University 2004 – 2006
- Vice Dean, Computer Science and Engineering, Chalmers, 2002 – 2004
- Vice Dean, Electrical & Computer Engineering, Chalmers, 1999 – 2002

Entrepreneurship Roles

- Founder of Nema Labs AB, 2007. CEO (2007-2009), member of the Board (2007-2012)
- Co-founder ZeroPoint Technologies, 2015. Chief Science Ofiicer (2015 –), member of the Board (2015 –)
- Co-founder InfiniNode Technologies, 2024. Member of the Board (2025 –).
- Scientific advisory board**.** I was on the scientific advisory board of EASE, Lund University between 2010-2014.
- Member of the board of Chalmers Innovation**.** I was on the Board of directors of Chalmers Innovation 2010 – 2015.

Honors & Awards

- IEEE Fellow, 2007 – 2024, IEEE Life Fellow, since 2024
- ACM Fellow, since 2008
- Member of the Royal Swedish Academy of Science, since 2009
- Member of the Academia Europaea, since 2010
- Member of the Royal Society of Arts and Sciences in Gothenburg, since 2016
- Fellow of the Asia-Pacific Artificial Intelligence Association (AAIA), since 2023
- Recipient of the 2021 ACM SIGARCH Alan D. Berenbaum Distinguished Service Award for the "creation and successful implementation of the TACO/HiPEAC journal-first review model, and for decades long exemplary service contributions to the field."
- Inducted to the Hall of Fame of the IEEE/ACM International Symposium on Computer Architecture (ISCA), 2005
- Inducted to the Hall of Fame of the IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2016
- HiPEAC Technology Transfer Award 2016
- HiPEAC Technology Transfer Award 2024
- 2020 IEEE TC Award for Editorial Service and Excellence as Topical Editor.
- Honorable mention as PhD supervisor of the year at Chalmers, 2021
- 2022 Selected on IVAs 100-list for Research2Business based on European Processor Initiative and ZeroPoint Innovations
- Biographical entry in The Marquis Who's Who in the World in the 12th-19th, 24th (2006) editions

Paper Awards

- H. Nilsson and P. Stenstrom: "An Adaptive Update-Based Cache Coherence Protocol for Reduction of Miss Rate and Traffic," In *Proceedings of PARLE (Parallel Architectures and Languages Europe)*, pp. 363-374, June 1994. Best Paper Award at the conference.
- P. Rundberg and P. Stenstrom: Low-Cost Thread-Level Data Dependence Speculation on Multiprocessors," in *4th Workshop on IEEE Multi-Threaded Execution, Architecture and Compilation (in conj. with Micro-33),* Dec 2000. (Received the Best Paper award.)
- H. Dybdahl, P. Stenstrom, L. Natvig, A Cache-Partition Aware Replacement Policy for Chip Multiprocessors. (Best Paper Award.) In *Proceedings of ACM 2006 HiPC*. December 2006.
- F. Warg and P. Stenstrom. Dual-Thread Speculation. Two Threads in the Machine is Better than Eight in the Bush. In *Proceedings of SBAC 2006*. (Best Paper Award) October 2006

- HiPEAC paper awards 2012, 2014, 2015, 2016, 2018 and 2022

Academic Genealogy

- **Emanuel Björling** (1839 – 1910) Professor of Mathematics, Lund University
- **Johannes Rydberg** (1854 – 1919), Professor of Physics, Lund University – widely known for Rydberg's formula and constant.
- **Karl Manne Siegbahn** (1886 – 1978), Professor of Physics, Lund University – Nobel Prize in Physics in 1924 for his discoveries in the field of X-ray Spectroscopy
- **Sten von Friesen** (1907 – 1996), Professor of Physics, Lund University – known for his discoveries in Nuclear Physics.
- **Hellmuth Hertz** (1920 – 1990), Professor of Electrical Measurement Technology, Lund University – known for his pioneering work on Inkjet and Ultrasound technology. His father got the Noble Prize in Physics in 1925 and his father's uncle, Heinrich Hertz, gave name to the unit Hertz for frequency.
- **Lars Philipson** (1945 – 2008), Professor of Computer Engineering, Lund University – known for his pioneering work on multiprocessor technology and making VLSI design a Swedish academic subject.
- **Per Stenström** (1957 –), Professor of Computer Architecture, Chalmers University of Technology, Alma Mater: Lund University – known for his pioneering contributions to the design of high-performance memory systems with innovations in cache coherency, latency tolerating techniques, memory and cache compression techniques and contributions to real-time systems, especially concerning the design of time-predictable computer architectures, a field he pioneered.

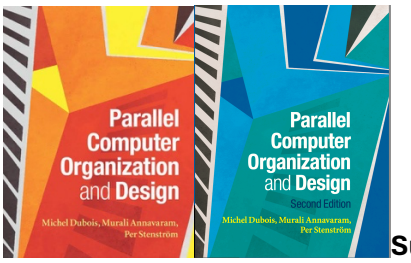
Pedagogical activities

Summary: My pedagogical experience spans more than 30 years and ranges from teaching and developing individual courses, including two MOOCs (Massive Open Online Courses at ChalmersX) and curricula development in terms of specializations and MSc programs. I am a deep fan of the flipped classroom methodology.

- I have taught courses on Digital Design, Computer Organization, Computer Architecture, and Parallel Computer Architecture over the past several decades.
- I'm author of four textbooks on Computer Organization and Assembly Language Programming and Parallel Computer Organization and Design
- Tutorials (PhD level): CNRS, France, 1994; ARTES, Stockholm, Sweden, 1998, iUPC Barcelona, 1998, 2002, Ericsson 1998, EuroPar95 and EuroPar97,
- Ph. D. course (24 hours) on shared-memory multiprocessors at UPC in Barcelona in April 2002.
- HiPEAC ACACES 2005. Course on chip-multiprocessor architecture.
- HiPEAC ACACES 2010 Course on "Methods to Transfer Research To Business" with Andrzej Brud of Chalmers Innovation.

- Ph. D. course on Advanced Topics in Computer Architecture, Beihang University in Beijing, Advanced Topics in Computer Architecture 2014.
- Ph. D. course on Compression in the Memory Hierarchy at UPMARC PhD summer school 2017.
- Ph. D course ACM Summer School, held in Barcelona in July 2019, 2022 and 2023 on Cache Coherency and Compression in the Memory Hierarchy.
- In 2016, I was asked to develop two MOOCs for Chalmers based on my courses: one basic and one advanced. This was one of the most inspiring tasks (and also laborious) I have done. Coached by the fantastic blended-learning team at Chalmers I developed first a basic course which centers on energy-efficient programming. It was launched at the edX platform in the fall of 2016. The second course, on advanced computer architecture, was launched on edX in January 2017. Both courses have been well-received and they have been delivered regularly under ChalmersX since then.
- Development of the MSc program High-Performance Computer Systems in 2017. The program was launched in 2019 and attracted 90 students in 2025.

Publications



Summary: My publication portfolio encompasses about 200 refereed scholarly publications appearing in top conferences and journals and more than 20 patents. I am author/co-author of 4 books of which I am most proud of "Parallel Computer Organization and Design".

Textbooks

1. L. Ohlsson and Per Stenström: "Computer Organization and Assembly Language Programming," Studentlitteratur and Chartwell-Bratt, ISBN 91-44-26461-5, January 1987.
2. Per Stenström: ''68000 Microcomputer Organization and Programming," Prentice-Hall, ISBN 0-13-584855-5, September 1992.
3. Michel Dubois Murali Annavaram, and Per Stenström. *Parallel Computer Organization and Design*. Cambridge Press. 1st Edition. 2013.
4. Somayeh Sardashti, Angelos Arelakis, Per Stenstrom, David Wood. A Primer on Compression in the Memory Hierarchy. Morgan-Claypool, 2015.
5. Michel Dubois Murali Annavaram, and Per Stenström. *Parallel Computer Organization and Design*. Cambridge Press. 2nd Edition. 2025.

Journal Papers

1. P. Stenström: “Reducing Contention in Shared-Memory Multiprocessors,” in *IEEE Computer*, Vol 21, No 11, pp. 26-37, November 1988.

2. P. Stenström: “A Survey of Cache Coherence Schemes for Multiprocessors,” in *IEEE Computer,* Vol 23, No 6, pp. 12-24, June 1990.

3. H. Grahn, P. Stenström, and M. Dubois: “Implementation and Evaluation of Update-Based Cache Protocols Under Relaxed Memory Consistency Models,” in *Future Generation Computer Systems*, Vol. 11, No. 3, pp. 247-271, June 1995.

4. F. Dahlgren and P. Stenström: “Using Write Caches to Improve Performance of Cache Coherence Protocols in Shared-Memory Multiprocessors,” in *Journal of Parallel and Distributed Computing*, Vol 26. No 2, pp. 193-210, April 1995.

5. F. Dahlgren, M. Dubois, and P. Stenström: “Sequential Hardware Prefetching in Shared-Memory Multiprocessors,” in *IEEE Trans. on Parallel and Distributed Systems,* Vol. 6 No 7, pp. 733-746, July 1995.

6. M. Dubois, J. Skeppstedt, and P. Stenström: “Essential Misses and Memory Traffic in Coherence Protocols,” in *Journal of Parallel and Distributed Computing*, Vol. 29, No 2, pp. 108-125, October 1995.

7. F. Dahlgren and P. Stenström “Evaluation of Stride and Sequential Hardware-based Prefetching in Shared-Memory Multiprocessors*,”* in *IEEE Trans. on Parallel and Distributed Systems,* Vol. 7, No. 4, pp. 385-398, April 1996.

8. M. Brorsson and P. Stenström: “Characterising and Modelling Shared-Memory Accesses in Multiprocessor Programs,” in *Parallel Computing*, No 22, pp. 869-893, 1996.

9. P. Stenström, M. Balldin, and J. Skeppstedt: “The Design of a Non-Blocking Load Processor Architecture,” in *Microprocessors and Microsystems, No 20, pp. 111-123,* 1996.

10. H. Grahn and P. Stenström: “Evaluation of an Adaptive Update-Based Cache Protocol,” in *Journal of Parallel and Distributed Computing*, 39(2):168-180, December 1996.

11. J. Skeppstedt and P. Stenstrom. Using Dataflow Analysis Techniques to Reduce Ownership Overhead in Cache Coherence Protocols. In *ACM Transactions on Computer Systems,* Vol. 18, No 6., pp. 659-682, November 1996

12. P. Stenström, M. Brorsson, F. Dahlgren, H. Grahn, and M. Dubois: “Boosting Performance of Shared-Memory Multiprocessors,” in *IEEE Computer,* pp. 63-70, July 1997.

13. M. Karlsson and P. Stenström: “Effectiveness of Dynamic Prefetching in Multiple-Writer Distributed Virtual Shared Memory Systems,” in *Journal of Parallel and Distributed Computing*, Vol. 43, No. 2, pp. 79-93, 1997.

14. F. Dahlgren, M. Björkman and P. Stenström: “Reducing the Read Miss Penalty for Flat COMA Protocols, in *the Computer Journal*, Vol. 40, No. 4, pp. 208-219, 1997.

15. P. Stenström, Erik Hagersten, David Lilja, Margaret Martonosi, and Madan Venugopal: “Trends in Shared-Memory Multiprocessing,” in *IEEE Computer,* Vol. 30, No. 12, pp. 44-50, December 1997.

16. F. Dahlgren, J. Skeppstedt, and P. Stenström: “An Evaluation of Hardware-Based and Compiler-Controlled Snooping Cache Protocol Extensions,” in *Journal of Future Generation Computer Systems,* No. 13, pp. 469-487,1998.

17. F. Dahlgren, M. Dubois, and P. Stenström: “Performance Evaluation and Cost Analysis of Cache Protocol Extensions for Shared-Memory Multiprocessors,” in *IEEE Transactions on Computers*, Vol. 47, No 10, pp. 1041-1055, Oct. 1998.

18. J. Skeppstedt, F. Dahlgren, and P. Stenström: “Evaluation of Compiler-Controlled Updating to Reduce Coherence-Miss Penalties in Shared-Memory Multiprocessors,” in *Journal of Parallel and Distributed Computing,* Vol. 56, No 2, pp. 122-153, 1999.

19. T. Lundqvist and P. Stenström: “An Integrated Path and Timing Analysis Method Based on Cycle-Level Symbolic Execution,” In *Journal of Real-Time Systems,* 17 (2/3):183-207, November 1999.

20. H. Grahn and P. Stenström: “Comparative Evaluation of Latency-Tolerating and Reducing Techniques for Hardware-Only and Software-Only Directory Protocols”, *Journal of Parallel and Distributed Computing,* Vol. 60, No. 7, pp. 807-834, July 2000.

21. J. Jalminger and P. Stenström “Improving Energy-Efficiency in Off-Chip Caches using Selective Prefetching”, In *Journal of Microprocessors and Microsystems*, No 26, pp. 107-121, 2002.

22. P. Rundberg and P. Stenström: An All-Software Thread-Level Data Dependence Speculation System for Multiprocessors,” *Journal of Instruction-Level Parallelism*, Vol 3. Oct 2002.

23. Håkan Grahn and Per Stenström. A Comparative Evaluation of Hardware-Only and Software-Only Directory Protocols in Shared-Memory Multiprocessors, *Journal of Systems Architecture*, Vol 50 (2004) pages 537-561.

24. Jonas Jalminger and Per Stenstrom: A Cache Block Reuse Prediction Scheme. *Journal of Microprocessors and Microsystems*. Vol 28 (2004), pages 373-385.

25. K. De Bosschere, G. Gaydadjiev, X. Martorell, N. Navarro, M. O’Boyle, D. Pnevmatikatos, A. Ramirez, P. Sainrat, A. Seznec, P. Stenstrom, and O. Temam. High-Performance Embedded Architecture and Compilation Roadmap. In *Transactions on High-Performance Embedded Architectures and Compilers*. Vol 1, No 3. Dec. 2006.

26. J. Chen, M. Dubois, and P. Stenstrom: Integrating Complete-system and User-level Performance/Power Simulators: the SimWattch Approach. In *IEEE Micro* Magazine, July-August, 2007.

27. J. Hollmann, A. Ardo, Per Stenstrom: The Effectiveness of Caching in a Distributed Digital Library. In *Journal of System Architecture,* pages 53(7) 403-416, 2007.

28. Mafijul Islam, Magnus Själander, and Per Stenstrom. Early Detection and Bypassing of Trivial Operations to Reduce Energy. in *Journal of Microprocessors and Microsystems*. October 2007.

29. Martin Thuresson, Magnus Själander, Magnus Björk, Lars Svensson, Per Larsson-Edefors, Per Stenstrom. FlexSoC: Utilizing Exposed Datapath Control for Efficient Computing. In *Journal of VLSI,* December 2007.

30. P. Stenstrom. The Paradigm Shift to Multi-Cores: Opportunities and Challenges. In Journal of *Applied and Computational Mathematics*. Vol 6, No 2, pages 253-257, 2007.

31. Reinhard Wilhelm, Jakob Engblom, Andreas Ermedahl, Niklas Holsti, Stephan Thesing, David B. Whalley, Guillem Bernat, Christian Ferdinand, Reinhold Heckmann, Tulika Mitra, Frank Mueller, Isabelle Puaut, Peter P. Puschner, Jan Staschulat, Per Stenstrom. The Determination of Worst-Case Execution Times — Overview of Methods and Survey of Tools. In *ACM Trans. Embedded Comput. Syst*. 7(3): (2008).

32. F. Warg and P. Stenstrom. Dual-Thread Speculation: A Simple Approach to Uncover Thread-Level Parallelism on a Simultaneous Multithreaded Processor. In *International Journal of Parallel Programming* 36(2): 166-183 (2008).

33. M. Thuresson, L. Spracklen, P. Stenstrom. Memory Link Compression Schemes: A Value Locality Perspective. In *IEEE Transactions on Computers*, Jan 2008.

34. Jaeheon Jeong, Per Stenstrom, and Michel Dubois. Simple Penalty-Sensitive Cache Replacement Policies. In *Journal of ILP*. Vol 10, July 2008.

35. J. Chen, Jianwei, M. Dubois, and P. Stenstrom, Per: SimWattch and Learn. In *IEEE Potentials*, 28 (1) pp. 17-23, 2009.

36. Etienne Riviere et al. The VELOX Transactional Memory Stack. In *IEEE Micro* Dec 2010.

37. A. Arelakis and P. Stenstrom. A Case for a Value-Aware Cache. In *IEEE Computer Architecture Letter*s. Issue 99, 2014.

38. A. Negi, R. Titos, M. Acacio, J. Garcia, P. Stenstrom. Eager beats Lazy: Improving Store Management in Eager Hardware Transactional Memory. In *IEEE Transactions on Parallel and Distributed Systems*. (to appear), 2012.

39. M. Islam and P. Stenstrom. Characterizing and Exploiting Small-Value Memory Instructions. In *IEEE Transactions on Computers*, 2013.

40. M. Flynn, O. Mencer, V. Milutinovic, G. Rakocevic, P. Stenstrom, R. Trobec, M. Valero. Viewpoint: Moving from PetaFlops to PetaData. In *ACM CACM,* May 2013.

41. R. Titos, A. Negi, M. Acacio, J. Garcia, P. Stenstrom. ZEBRA: Data-Centric Contention Management in Hardware Transactional Memory. In *IEEE Transactions on Parallel and Distributed Systems*. 2013.

42. M.M. Waliullah and P. Stenstrom. Removal of Conflicts in Hardware Transactional Memory Systems. In *Int. Journal of Parallel Programming (IJPP)*. 42(1): 198-218 (2014)

43. Minghua Li, Guancheng (G.C.) Chen, Qijun Wang, Yong Hua Lin, Per Stenstrom, Peter Hofstee, Dian Zhou PATer: A Hardware Prefetching Automatic Tuner on IBM POWER8 Processor. In *IEEE Computer Architecture Letters*. 2015

44. M. Manivannan, M. Pericàs, V. Papaefstathiou, P. Stenstrom. Runtime-Assisted Global Cache Management for Task-based Parallel Programs. In *IEEE Computer Architecture Letters*. 2016.

45. M. Waqar Azhar, P. Stenstrom, V. Papaefsthatiou. SLOOP: QoS-Supervised Loop Execution to Reduce Energy on Heterogeneous Architectures. In *ACM Transactions on Architecture and Code Optimization (TACO)*. 2017.

46. A. Angerd, E. Sintorn, P. Stenstrom. A Framework for Automated and Controlled Floating-Point Accuracy Reduction in Graphics Applications on GPUs. In *ACM Transactions on Architecture and Code Optimization (TACO)*. 2017.

47. R. Pathan, P. Voudouris, P. Stenstrom. Scheduling Parallel Real-Time Recurrent Tasks on Multicore Platforms. In *IEEE Transactions on Parallel and Distributed Systems*. Vol 4, No 29, pp. 915-928, 2018.

48. Madhavan Manivannan, Miquel Pericàs, Vassilis Papaefstathiou, Per Stenstrom. Global Dead-Block Management for Task-Parallel Programs. In *ACM Transactions on Architecture and Code Optimization (TACO)*. 2018.

49. Mehrzad Nejat, Madhavan Manivannan, Miquel Pericàs, Per Stenstrom: Coordinated Management of DVFS and Cache Partitioning under QoS Constraints to Save Energy in Multi-Core Systems. In *Journal of Parallel and Distributed Systems*. 2020.

50. P. Voudouris, P. Stenstrom, R. Pathan. Federated Scheduling of Sporadic DAGs on Unrelated Multiprocessors. In *ACM Trans. Embed Comput. Syst*. 20, 1-25, 2021.

51. Petros Voudouris, Per Stenstrom, Risat Pathan. Bounding the Execution Time of Parallel Applications". In *Real-time Systems Journal*. 2022.

52. M. W. Azhar, M. Pericás, P. Stenstrom. Task-RM. A Resource Manager for Energy Reduction in Task-Parallel Applications under Quality of Service Constraints. In *ACM Transactions on Architecture and Code Optimization*. 2022.

53. M. Nejat, M. Manivannan, M. Pericàs, P. Stenstrom. Cooperative Slack Management: Saving Energy of Multi-Core Processors by Trading Performance Slack Between QoS Constrained Application. In *ACM Transactions on Architecture and Code Optimization*. 2022.

54. M. W. Azhar, M. Mannivanan, P. Stenstrom. Approx-RM: Reducing Energy on Heterogeneous Multicore Processors under Accuracy and Timing Constraints. In *ACM Transactions on Architecture and Code Optimization*. 2023.

55. Qi Shao and Per Stenstrom. CrossFetch: A Prefetching Scheme for Cross-Page Prefetching in the Physical Address Space. Accepted for publication in *IEEE Computer Architecture Letters.* December 2025.

Conference Papers (refereed)

- **Note: in Computer Architecture/Science the publication culture is such that it favors dissemination of full papers in conferences.**

1. P. Stenström and L. Philipson: "A layered emulator for design evaluation of MIMD multiprocessors with shared memory," in *Proc. of PARLE (Parallel Architectures and Languages Europe)*, Lecture Notes in Computer Science, No 258, Springer-Verlag, pp. 329-344, June 1987.

2. P. Stenström: "VLSI Support for a Cactus Stack Oriented Memory Organization," in *Proc. of the 21st Hawaii International Conference on System Sciences*, pp. 211-220, January 1988.

3. P. Stenström, D. Vrsalovic, and Z. Segall: "Shared Data Structures in a Distributed System — Performance Evaluation and Practical Considerations," in *Proc. of IFIP TC 7/WG 7.3, International Seminar on Performance of Distributed and Parallel Systems*, pp. 15-30, December 1988.

4. P. Stenström: "A Cache Consistency Protocol for Multiprocessors with Multistage Networks," in *Proc. of 16th Annual International Symposium on Computer Architecture*, pp. 407-415, May 1989.

5. P. Stenström, F. Dahlgren, and L. Lundberg: "A Lockup-free Multiprocessor Cache Design," in *Proc. of International Conference on Parallel Processing*, Vol 1, pp 246-250, August 1991.

6. F. Dahlgren and P. Stenström: "On Reconfigurable On-chip Data Caches," in *Proc. of 24th ACM/IEEE International Symposium on Microarchitectur*e, pp. 189-198, November 1991.

7. F. Dahlgren and P. Stenström: "Reducing Write Latencies for Shared Data in a Multiprocessor with a Multistage Network," in *Proc. of 25th Hawaii International Conference on System Sciences*, pp. 449-456, January 1992.

8. P. Stenström: "A Latency-Hiding Scheme for Multiprocessors with Buffered Multistage Networks," in *Proc. of International Parallel Processing Symposium*, pp. 39-42, March 1992.

9. P. Stenström, T. Joe, and A. Gupta: "Comparative Performance Evaluation of Cache-Coherent NUMA and COMA Architectures," in *Proc. of 19th Annual International Symposium on Computer Architecture*, pp. 80-91, May 1992.

10. H. Nilsson and P. Stenström: "The Scalable Tree Protocol — A Cache Coherence Approach for Large-Scale Multiprocessors," in *Proc. of Fourth IEEE Symposium on Parallel and Distributed Processing*, pp. 498-507, December 1992.

11. M. Brorsson and P. Stenström: "Visualising Sharing Behaviour and its Relation to Shared Memory Management," in *Proc. of 1992 International Conference on Parallel and Distributed Systems*, pp. 528-536, December 1992.

12. H. Nilsson and P. Stenström: “Performance Evaluation of Link-Based Cache Coherence Schemes,” in *Proc. of 26th Hawaii International. Conference on System Sciences*, pp. 486-495, January 1993.

13. P. Stenström, H. Nilsson, and J. Skeppstedt: “Using Graphics and Animation to Visualize Instruction Pipelining and its Hazards,” in *Proc. of ICSEE'93*, pp. 130-135 January 1993.

14. M. Brorsson, F. Dahlgren, H. Nilsson, and P. Stenström: “The CacheMire Test Bench—A Flexible and Effective Approach for Simulation of Multiprocessors,” in *Proc. of 26th IEEE Annual Simulation Symposium*, pp. 41-49, March 1993.

15. P. Stenström, M. Brorsson, and L. Sandberg: “An Adaptive Cache Coherence Protocol Optimized for Migratory Sharing,” in *Proc. of 20th ACM/IEEE Annual International Symposium on Computer Architecture*, pp. 109-118, May 1993.

16. M. Dubois, J. Skeppstedt, L. Ricciulli, K. Ramamurthy, and P. Stenström: The Detection and Elimination of Useless Misses in Multiprocessors. In *Proc. of 20th ACM/IEEE Annual International Symposium on Computer Architecture*, pp. 88-97, May 1993.

17. F. Dahlgren, M. Dubois, and P. Stenström: Fixed and Adaptive Sequential Prefetching for Shared-Memory Multiprocessors. In *Proc. of 1993 International Conference on Parallel Processing*, pp. 56-63, August 1993.

18. F. Dahlgren, M. Dubois, and P. Stenström: Combined Performance Gains of Simple Cache Protocol Extensions. In *Proc. of 21st ACM/IEEE Annual International Symposium on Computer Architecture*, pp. 187-197, April 1994.

19. H. Nilsson and P. Stenström: An Adaptive Update-Based Cache Coherence Protocol for Reduction of Miss Rate and Traffic. In *Proc. of PARLE (Parallel Architectures and Languages Europe)*, pp. 363-374, June 1994. Best Paper Award at the conference.

20. F. Pong, P. Stenström, and M. Dubois: An Integrated Methodology for Verification of Correctness of Cache Coherence Protocols. In *Proc. of 1994 International Conference on Parallel Processing*, pp. 158-165, August 1994.

21. F. Dahlgren and P. Stenström: Reducing the Write Traffic for a Hybrid Cache Protocol. In *Proc. of 1994 International Conference on Parallel Processing*, pp. 166-173, August 1994.

22. J. Skeppstedt and P. Stenström. Simple Compiler Algorithms to Reduce Ownership Overhead in Cache Coherence Protocols. In *Proc. of 6th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS VI*), pp. 286-296, October 1994.

23. M. Brorsson and P. Stenström. Modelling Accesses to Stationary Data in Shared Memory Multiprocessors. In *Proc. of the 7th International Conference on Parallel and Distributed Computing (PDCS'94)*, pp. 802-807, October 1994.

24. M. Brorsson and P. Stenström. Modelling Accesses to Migratory and Producer-Consumer Characterised Data in a Shared Memory Multiprocessor. In *Proc. of*

Sixth IEEE Symposium on Parallel and Distributed Processing, pp. 612-619, October 1994.

25. M. Björkman, F. Dahlgren, and P. Stenström. Using Hints to Reduce Read Miss Penalties for Flat COMA Protocol. In *Proc. of 28th Hawaii International Conference on System Sciences,* pp. 242-251, January 1995.

26. F. Dahlgren and P. Stenström. Effectiveness of Stride and Sequential Hardware-based Prefetching in Shared-Memory Multiprocessors. In *Proc. of First International Conference on High Performance Computer Architecture (HPCA-1)*, pp. 68-77, January 1995.

27. H. Grahn and P. Stenström. Efficient Strategies for Software-Only Directory Protocols in Shared-Memory Multiprocessors. In *Proc. of 22nd ACM/IEEE Annual International Symposium on Computer Architecture*, pp. 38-47, June 1995.

28. J. Skeppstedt and P. Stenström. A Compiler Algorithm that Reduces Read Latency in Ownership-Based Cache Coherence Protocols. In *Proc. of Parallel Architectures and Compilation Techniques,* pp. 69-78, July 1995.

29. F. Dahlgren, J. Skeppstedt, and P. Stenström. Effectiveness of Hardware-Based and Compiler-Controlled Snooping Protocol Extensions. In *Proc. of the International Conference on High Performance Computing, pages 87-92,* December 1995.

30. M. Karlsson and P. Stenström: "Performance Evaluation of a Cluster-Based Multiprocessor Built from ATM-Switches and Bus-Based Multiprocessor Servers," in *Proc. of Second International Conference on High Performance Computer Architecture*, pages 4-13, Jan. 1996.

31. H. Grahn and P. Stenström: "Relative Performance of Software-Only and Hardware-Only Directory Protocols Under Latency Tolerating and Reducing Techniques," in *Proceedings of the 11th International Parallel Processing Symposium*, pages 500-506, April 1997.

32. P. Stenström and J. Skeppstedt: "A Performance Tuning Approach for Shared-Memory Multiprocessors" in *Proceedings of EUROPAR'97*, pp. 72-84, August 1997.

33. J. Nilsson, F. Dahlgren, M. Karlsson, P. Magnusson, P. Stenström: "Computer System Evaluation with Commercial Workloads" in *Proc. of IASTED Conference on Modeling and Simulation*. pp. 293-297, May 1998.

34. P Magnusson, F Dahlgren, H. Grahn, M. Karlsson, F. Larsson, A. Moestedt, J. Nilsson, P Stenström, and B. Werner: "SimICS/Sun4m: A Virtual Workstation. In *Proc. of USENIX98,*pp. 119-130, June 1998.

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5. V. Milutinovic and P. Stenström “Opportunities and Challenges for Distributed Shared-Memory Multiprocessors. Guest Editors’ Introduction, *Proceedings of the IEEE*. Vol 87 No 3, pp 399-404, March 1999.

6. S. Muller, P. Stenström, M. Valero, and S. Vassiliadis: “Parallel Computer Architecture”, in *Proc. of EUROPAR’00,* Aug. 2000.

7. Proceedings of the 2003 ACM Conference on Languages, Tools & Compilers for Embedded Computer Systems, editors Frank Mueller and Per Stenström. San Diego June 2003.

8. Proceedings of the 2004 IEEE/ACM Proceedings of the 31st International Symposium on Computer Architecture, editors Michel Dubois, Arndt Bode, and Per Stenström. Munich, June 2004.

9. F. Mueller and P. Stenstrom. Introduction to Special Issue on “Languages, Compilers, and Tools for Embedded Systems,” in *ACM Trans. on Embedded Computer Systems.* 2005.

A. Monien, G. Gao, H. Simon, P. Spirakis, P. Stenstrom. Introduction to Special Issue on “2004 International Parallel and Distributed Processing Symposium” in *Journal of Parallel and Distributed Computing*. 2005.

10. P. Stenstrom, M. O’Boyle, F. Bodin, M. Cintra, Sally A. McKee (eds). *Transactions on HiPEAC,* Vol 1. Springer Verlag, 2007

11. K. De Bosschere, D. Kaeli, P. Stenstrom, T. Ungerer, D. Whalley (eds). *Proceedings of the 2007 International Conference on HiPEAC.* Springer Verlag, January, 2007.

12. M. Dubois and P. Stenstrom (eds). *Proceedings of the 2007 ACM International Conference on Computing Frontiers.* May 2007.

13. P. Stenstrom, M. Dubois, M. Katevenis, and R. Gupta (eds). *Proceedings of the 2008 International Conference on HiPEAC.* Springer Verlag, January, 2008

14. J. Carter, A. Gonzalez, and P. Stenstrom (eds). *Proceedings of the 2008 IEEE International Symposium on High-Performance Computer Architecture.* February 2008.

A. Mei and P. Stenstrom (eds) *Proceedings of the 2009 IEEE International Parallel & Distributed Processing Symposium. May 2009.*

15. P. Stenstrom (eds). Transactions on High-Performance Architectures and Compilers. Vol 2, 2009.

16. P. Stenstrom (eds). Transactions on High-Performance Architectures and Compilers. Vol 3, 2011.

17. P. Stenstrom (eds). Transactions on High-Performance Architectures and Compilers. Vol 4, 2011.

18. P. Stenstrom, Koen De Bosschere (eds.) Special issue on High-Performance and Embedded Architectures and Compilers. In *ACM TACO Vol. X No 1. 2012.*

19. P. Stenstrom, Koen De Bosschere (eds.) Special issue on High-Performance and Embedded Architectures and Compilers. In *ACM TACO Vol. X No 1. 2013.*

20. P. Stenstrom, Koen De Bosschere (eds.) Special issue on High-Performance and Embedded Architectures and Compilers. In *ACM TACO Vol. X No 1. 2014.*

21. Yves Robert, V. Prasanna, P. Stenstrom. What's Next. Guest Editors' Introduction to a Special issue. Journal of Parallel and Distributed Computing, 74(6), 2014.

22. A. Bode, M. Gerndt, P Stenstrom (eds). Proceedings of 2014 ACM International Conference on Supercomputing.

23. P. Stenstrom. 2015. In IEEE Micro April 2016.

24. S. Evripidou, M. O'Boyle, P. Stenstrom (eds). Proceedings of the 27th ACM/IEEE Parallel Architectures and Compilation Techniques. 2018.

25. P-C Yew, P. Stenstrom, J. Wu, X Gong, T Li (eds): Advanced Parallel Processing Technologies – 13th Int. Symp. APPT, 2019, Tianjin, China.

Selected Tech. Reports

1. P. Stenström: "*MUMS Processing Element: Hardware Design,"* Technical Report, Department of Computer Engineering, Lund University, June 1987.

2. P. Stenström: "*MUMS Processing Element: Architecture Manual,"* Technical Report, Department of Computer Engineering, Lund University, June 1987.

3. P. Stenström: "*Sequentially Consistent, Packet-Switched, Multiprocessor Memory Systems,"* Technical Report, Department of Computer Engineering, Lund University, March 1990.

4. A. Gupta, T. Joe, and P. Stenström. "*Performance Limitations of Cache-Coherent NUMA and Hierarchical COMA Architectures and the Flat-COMA Solution* Technical Report CSL-TR-92-524, Computer Systems Laboratory, Stanford University, October 1992

5. F. Pong, P. Stenström, M. Dubois, "*An Integrated Methodology for the Verification of Directory-Based Cache Protocols,"* USC Tech. report, November 1994.

Reprints in Tutorials

1. The paper "A Survey of Cache Coherence Schemes for Multiprocessors," originally published in *IEEE Computer*, Vol 23, No 6, pp. 12-24, June 1990 has been reprinted in "The Cache Coherence Problem in Shared-Memory Multiprocessors: Hardware Solutions," IEEE Computer Society Press, M Tomasevic and V. Milutinovic, 1993.
2. The paper "Comparative Performance Evaluation of Cache-Coherent NUMA and COMA Architectures," originally published in *Proc. of 19th Annual International Symposium on Computer Architecture*, pp. 80-91, May 1992 has been reprinted in "The Cache Coherence Problem in Shared-Memory Multiprocessors: Hardware Solutions," IEEE Computer Society Press, M Tomasevic and V. Milutinovic, 1993.
3. The paper "Comparative Performance Evaluation of Cache-Coherent NUMA and COMA Architectures," originally published in *Proc. of 19th Annual International Symposium on Computer Architecture*, pp. 80-91, May 1992 has been reprinted in "Multiprocessor Performance Measurement and Evaluation," IEEE Computer Society Press, L Bhuyan and X. Zhang, 1995.

Patents

- **Summary:** 23 patent families; 97 submitted patents of which 68 have been granted (2024)
- *Multiprocessorsystem för att minska effektförbrukningen hos logik i förbindelser med processorer i systemet*. Filed 16 November, 2001 (in Sweden); March 1, 2003 (in the U.S.). Issued on April 6, 2004 (in Sweden). Published (20030115402) Co-inventors: Magnus Ekman and Fredrik Dahlgren.
- *Coherence message prediction mechanism and multiprocessing computer system employing the same*. Inventors: Jim Nilsson, Anders Landin, Per Stenstrom. Filed by Sun Microsystems to U.S. Patent Office, April 18, 2003. Issued on Dec 6, 2005 as US Patent 6,973,547.
- *Cache Coherency Protocol Including Generic Transient States*. Filed by Sun Microsystems to U.S. Patent Office, Inventor: Per Stenstrom, March 2004. Published (20050210203). Issued on March 22, 2008. US Patent 7,350,032
- *System and Method for Coherence Prediction*. Filed by Sun Microsystems to U.S. Patent Office. Inventor: Per Stenstrom. Filed May 2005. Issued on April 24, 2008. U.S. Patent 7,363,435
- *Method and system for managing process memory configured in resizable uncompressed and compressed regions*. Filed by Sun Microsystems to U.S. Patent Office, September 2004. Issued on September 8, 2009 as US Patent 7,587572. Inventor: Per Stenstrom.
- *Generating and Comparing Memory Access Ranges for Speculative Throughput Computing.* Filed as a utility patent by Nema Labs AB to U.S. Patent Office and PCT through European Patent Office, January 2008. Issued on March 16, 2010 as US Patent 7,681,015 Inventors: Alexander Busck, Mikael Engbom, Per Stenstrom, Fredrik Warg.
- *System and Method for Memory Compression.* Filed by Sun Microsystems to U.S. Patent Office, September 9, 2005. Issued on April 20, 2010 as US Patent 7,702,875. Inventors: Magnus Ekman and Per Stenstrom.
- *Method and mechanism for cache compaction and bandwidth reduction*. Filed by Oracle America Inc., August 4, 2005. Issued on October 25, 2011 as US Patent 8,046,538. Inventor: Per Stenstrom
- Methods and Systems for a Compressed Cache, Angelos Arelakis and Per Stenstrom. 2024
- HMComp: Extending Near-Memory Capacity using Compression in Hybrid Memory, Qi Shao, Angelos Arelakis, Per Stenstrom. 2024
- Memory management for Compressed Memories, Anders Persson, Alexandra Angerd, Angelos Arelakis, Daniel Moreau, Pedro Moura Trancoso, Yiannis Nikolakopoulos, Per Stenstrom, PCT/SE2024/051075. 2023
- Identification of random-access pages and mitigation of thei impact on compressible computer memories, Evangelos Vasilakis, Angelos Arelakis, Vasileios Spiliopoulos, Per Stenstrom, Granted under SE545356. 2022
- Systems, methods and devices for exploiting value similarity in computer memories, Alexandra Angerd, Angelos Arelakis, Erik Sintorn, Per Stenstrom, WO2022119493, Granted under SE544557. 2020

- Variable-sized symbol entropy-based data compression. Inventor: Per Stenstrom. 2020. Filed at Swedish Patent Office (PRV) on March 31, 2016. Issued on May 26, 2020. Assigned to ZeroPoint Technologies.
- Systems, methods and devices for eliminating duplicates and value redundancy in computer memories, Angelos Arelakis, Per Stenstrom, WO2020145874, Granted under SE543186, EP3908938, IN556274, JP7571026, US12124420. 2019
- Methods, devices and systems for efficient compression and decompression for higher throughput, Henrik Häggebrant, Daniel Moreau, Angelos Arelakis, Per Stenstrom, WO2020130929, Granted under ZL2019800848115, HK40051574, US11658679. 2018
- Accessing compressed computer memory, Angelos Arelakis, Vasilis Spiliopoulos, Per Stenstrom, WO2020101564, Granted under SE544272, EP3881187, CN113015966, US11868271.
- Managing free space in a compressed memory system, Chloe Alverti, Angelos Arelakis, Ioannis Nikolakopoulos, Per Stenstrom, Pedro Trancoso, WO2020101562, Granted under SE543649, EP3881188, ZL2024091600186570, US11922016. 2018
- Methods, devices and systems for compressing and decompressing data, Angelos Arelakis, Per Stenstrom, WO2017131579, Granted under US10831655 and CN108886367. 2017
- Methods, devices and systems for compressing and decompressing data, Angelos Arelakis, Per Stenstrom, WO2017131578, Granted under US10846218, SE540178 and CN108702160. 2017
- Methods, devices and systems for semantic-value data compression and decompression, Angelos Arelakis, Per Stenstrom, WO 2016186564 A1, Granted under US10268380, JP7031828, CN107836083, EP4012928, EP3298695, EP602016068113.7, ZL2016800394960, HK40056158, KR10-2616804. 2016
- Methods, devices and systems for hybrid data compression and decompression, Angelos Arelakis, Per Stenstrom, WO 2016186563 A1, Granted under US10476520, US10819369, EP602016055730.4, EP3304746, JP7010548 and CN107925418, IN503169, KR 10-2578689. 3/92024 2022 2022 2016 Cache system and a method of operating a cache memory, Angelos Arelakis, Per Stenstrom, Granted under US9330001. 2016
- Cache system and a method of operating a cache memory, Angelos Arelakis, Per Stenstrom, Granted under US9330001. 2016

Graduated PhDs

- **Summary:** I have had more than 20 PhD students who have got their degree under my supervision. I have taken supervision very seriously meaning working with the students on a day-per-day basis.

1. Mats Brorsson: *"Performance Impact of Shared Memory Latency in Multiprocessors: Models and Experiments,"* Ph. D. thesis, (main advisor, co-supervised by Lars Philipson) Department of Computer Engineering, Lund University, May 1994. First employment Assist. prof. Lund Univeristy

2. Fredrik Dahlgren: *"Design and Performance Evaluation of Hardware-Based Cache Protocol Extensions for Multiprocessors,"* Ph. D. thesis, (main advisor) Department of Computer Engineering, Lund University, November 1994. First employment: Assist. res. prof. Lund University.
3. Håkan Grahn: "*Evaluation of Design Alternatives for a Directory-Based Cache Coherence Protocol in Shared-Memory Multiprocessors,*" Ph. D. thesis, (main advisor) Department of Computer Engineering, Lund University, December 1995. First employment: Assist. prof. University of Karlskrona/Ronneby.
4. Jonas Skeppstedt: "*Compiler Based Approaches to Reduce Memory Access Penalties in Cache-Coherent Multiprocessors,*" Ph. D. thesis (main advisor), Department of Computer Engineering, Chalmers University of Technology, May 1997. First employment: Assist. prof., Halmstad University.
5. Magnus Karlsson: "*Data Prefetching Techniques Targeting Single and a Network of Processing Nodes*". Ph. D. thesis (main advisor), Department of Computer Engineering, Chalmers University of Technology, December 1999. First employment: Hewlett Packard Laboratories, Palo Alto.
6. Ashley Saulsbury: "*Attacking Latency Bottlenecks in Distributed Shared Memory Systems,"* Ph.D. thesis (co-advised with Prof. Seif Haridi), Department of Teleinformatics, the Royal Institute of Technology, Stockholm, December 1999. First employment: Sun Microsystems, Menlo Park.
7. Thomas Lundqvist: "*A WCET Analysis Method for Pipelined Microprocessors and Cache Memories",* Ph. D. thesis (main advisor), Department of Computer Engineering, Chalmers University of Technology, June 2002. First employment: Lecturer at University College West.
8. Jim Nilsson: "*Towards Accurate and Resource-Efficient Coherence Prediction*" Ph. D. thesis (main advisor), Department of Computer Science and Engineering, Chalmers University of Techology, January 2004. First Employment: Startup company.
9. Magnus Ekman: "*Strategies to Reduce Energy and Cost of Chip Multiprocessor Systems,"* Ph. D. thesis (main advisor), Department of Computer Science and Engineering, Chalmers University of Technology, December 2004. First employment: Sun Microsystems.
10. Fredrik Warg: "*Techniques to Reduce Thread-Level Speculation Overhead,"* Ph. D. thesis (main advisor), Department of Computer Science and Engineering, Chalmers University of Techology, June 2006. First employment: Nema Labs (startup company).
11. Martin Thuresson: "Compression Techniques for Improved Bandwidth and Static Code Size in Computer Systems". Ph. D. thesis (main advisor). Department of Computer Science and Engineering, Chalmers University of Techology, September 2008. First employment: Google.
12. M. M. Waliullah. "*Performance Optimization Techniques for Hardware Transactional Memory*" Ph. D. thesis (main advisor). Department of Computer Science and Engineering, Chalmers University of Techology, February 2011. First employment: NVIDIA, California, U.S.
13. Mafijul Md. Islam. "*Techniques to Cancel Execution Early to Improve Processor Efficiency*". Ph. D thesis (main advisor). Department of Computer Science and

Engineering, Chalmers University of Technology, June 2011. First employment: Volvo Technology.

14. Anurag Negi. "*Speculative State and Contention Management in Hardware Transactional Memory*". Ph. D. thesis (main advisor). Department of Computer Science and Engineering, Chalmers University of Technology, March 2013. First employment. NVIDIA. Portland, Oregon, U.S.A.
15. Angelos Arelakis. "*Statistical Compression Cache Designs*" Ph.D. thesis (main advisor). Department of Computer Science and Engineering, Chalmers University of Technology, October 2015. First employment: Chalmers University of Technology, Göteborg, Sweden.
16. Andreas de Blanche "*A Slowdown Prediction Method to Improve Memory Aware Scheduling*" Ph.D thesis (examiner and co-supervisor; main advisor Stefan Christiernin) Department of Computer Science and Engineering, Chalmers University of Technology, May 2016.
17. Madhavan Manivannan "*Runtime-Assisted Cache Management using Dependency Annotations*" Ph.D. thesis (main advisor), Department of Computer Science and Engineering, Chalmers University of Technology, June 2016. First employment: startup company.
18. Dmitry Knyaginin "*Towards Large-Capacity and Cost-Effective Main Memories*" Ph.D. thesis (main advisor; co-supervised by Georgi Gaydadjiev and Vassilis Papaefstathiou), Department of Computer Science and Engineering, Chalmers University of Technology, May 2017. First employment: Qamcom.
19. Alexandra Angerd "*Approximation and Compression Techniques to Enhance Performance of Graphics Processing Units*" (main advisor; co-supervised by Erik Sintorn), Department of Computer Science and Engineering, Chalmers University of Technology, January 2021. First employment: ZeroPoint Technologies
20. Petros Voudouris "*Scheduling techniques to improve the worst-case execution time of real-time parallel applications on heterogeneous platforms*" (main advisor, co-supervised by Risat Pathan). Department of Computer Science and Engineering, Chalmers University of Technology, May 2021.
21. Muhammad Waqar Azhar. "*Techniques to Improve Energy Efficiency on Heterogeneous Multiprocessors under Timing and Quality Constraints*" (main advisor, co-supervised with Miquel Pericàs, Vassilis Papaefsthatiou and Madhavan Manivannan). Department of Computer Science and Engineering, Chalmers University of Technology. March 2022.
22. Mehrzad Nejat. "Dynamic Management of Multi-Core Processor Resources to Improve Energy Efficiency under Quality-of-Service Constraints" (main advisor; co-supervised with Miquel Pericàs and Madhavan Manivannan). Department of Computer Science and Engineering, Chalmers University of Technology. May 2022
23. Nadja Ramhoj Holtryd "Adaptive Microarchitectural Optimizations to Improve Performance and Security of Multi-Core Architectures" (main advisor; co-supervised with Miquel Pericàs and Madhavan Manivannan) Department of Computer Science and Engineering, Chalmers University of Technology. February 2023

Graduated Licentiates of Technology

1. Magnus Broberg: "*An Approach to Tune Performance of Multithreaded Programs on Multiprocessors*," Licentiate thesis (examiner, main advisor: Lars Lundberg), Department of Computer Science, University of Karlskrona/Ronneby, June 1999.
2. Ulf Assarsson: "*View Frustum Culling and Animated Ray Tracing: Improvements and Methodological Considerations"*, Licentiate thesis (main advisor, co-advised by Dr. Tomas Möller). May 2001.
3. Jonas Jalminger. "*On Improving Data Cache Space Utilization*", Licentiate thesis (main advisor), Jan 2002.
4. Martin Kampe. "*Prediction Methods for Cache and Branch Management in Computers,* Licentiate thesis (main advisor, co-advised by Dr. Fredrik Dahlgren, and Prof. Michel Dubois), May 2002.
5. Peter Rundberg. "*Data Dependence Speculation Methods to Expose Thread-Level Parallelism* (main advisor), Nov 2002.
6. Jochen Hollman "*Latency Reduction and Tolerance in Distributed Digital Libraries*" (main advisor, co-advised by Dr. Anders Ardö) Sept 2003
7. Nima Namaki. *"Dominated Performance: Methodology, Tools and Empirical Experiments*. (main advisor, co-advised by Stefan Christiernin), December 2008.
8. Qi Shao. "*Techniques to Expand Capacity in Memory Hierarchies using Compression"* (main advisor), April 2025.
9. Piyumal Ranawaka. "*Techniques to Improve Management of On-Chip Memories of Deep Learning Accelerators"* (main advisor), August 2025.

Postdoctoral Student Supervision

- Rubén Gonzalez (2010 – 2012)
- Rubén Titos (2012 – 2014)
- Miquel Pericas (2014 – 2016)
- Vassilis Papaefstathiou (2014 – 2016)
- Risat Pathan (2014 – 2016)
- Madhavan Manivannan (2018 –2022, now research engineer)
- Bhavishya Goel (2019 –2022, now research engineer)
- Mehrzad Nejat (2022 –2025)

Professional Service

Editorship

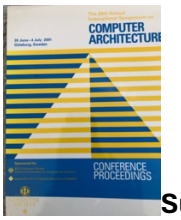
- **Summary:** I have acted as editor for seven journals and as Editor-in-Chief for two.
- Associate Editor-in-Chief (Computer Architecture) for Journal of Parallel and Distributed Computing, 2011 – 2025.
- Associate and Topical Editor of IEEE Transactions on Computers, 2019 – 2025

- Senior Associate Editor ACM *Transactions on Architecture and Code Optimization* (TACO), 2011 – 2025.
- Editor of *IEEE Micro*, 2016 – 2020.
- Editor (area: shared-memory multiprocessors) for JPDC (*Journal of Parallel and Distributed Computing*) 1993-2011.
- Editor-in-chief, *Transactions on High-Performance Embedded Architectures and Compilers*, 2004-2010
- Editor of *IEEE Transactions on Parallel and Distributed Systems*, 2008- 2011.
- Editor of the *International Journal of Embedded Systems,* 2004-2009.
- Editor of IEEE/TCCA *Computer Architecture Letters,* 2001-2010.
- Editor of *IEEE Transaction on Computers*, 2000-2004

Guest Editorship

- **Summary:** I have guest edited eight issues with colleagues.
- Guest editor for "Applications for Shared-Memory Multiprocessors" in the December 1996 issue of *IEEE Computer* together with Dr. Fredrik Dahlgren.
- Guest editor for "Distributed Shared-Memory Multiprocessors" in the Spring issue 1999 of the *Proceedings of the IEEE* together with Dr. Veljko Milutinovic.
- Guest editor for "Languages, Compilers, and Tools for Embedded Systems" in *ACM Transaction on Embedded Computer Systems* in March, 2004 together with Dr. Frank Mueller.
- Guest editor for "*Transactions on HiPEAC*" top papers in 2005 International Conference on High-Performance Embedded Architectures and Compilers, March 2006.
- Guest editor for "*Transactions on HiPEAC*" top papers in 2007 International Conference on High-Performance Embedded Architectures and Compilers, March 2007.
- Guest editor (together with Viktor Prasanna and Yves Robert) on a special issue in *Journal of Parallel and Distributed Processing* (scheduled for publication in JPDC 74(6), 2014) on What's Next.
- Guest editor for a special issue in *Journal of Parallel and Distributed Processing* "Trends on Heterogeneous and Innovative Hardware and Software Systems" Sanjay Ranka, Eduard Ayguade, Per Stenstrom, Jesus Carretero and Alba Melo, 2018
- Guest editor with Onur Mutlu on a Special Issue in *IEEE Transactions on Computers* on In/Near-memory processing scheduled for October 2023

Conference chair



Summary: I have acted as conference chair for 26 venues. I am most proud of having been general and program chair for the International Symposium on Computer Architecture (ISCA)

- Program vice-chair, 14th *IEEE Symp. on Distributed Computer Systems*, 1994
- Minitrack coordinator for "Shared Memory Multiprocessors" in the 27th Hawaiian International Conference on System Sciences, 1994.
- Global chair for the Parallel Computer Architecture Topic of *Euro-Par'96* and *2000*.
- General chair for the *28th IEEE/ACM Annual International Symposium on Computer Architecture* held Gothenburg, July 2-4,2001
- Program chair of *ACM/SIGPLAN LCTES'2003* (Languages, Tools & Compilers for Embedded Systems).
- Program vice-chair of Architecture Track of 2004 *IEEE International Parallel and Distributed Processing Symposium*.
- Program chair of 31st IEEE/ACM *Annual International Symposium on Computer Architecture* held in Munich, 2004.
- Program vice-chair of the Architecture track of the *2004 ACM Conference on High-Performance Computing*.
- Program track chair of the High-Performance Embedded Processor Architecture Track of the *2005 ACM Computing Frontier Conference*.
- Program co-chair of 2007 *High-Performance Embedded Architecture and Compiler Conference* (HiPEAC).
- Program co-chair of 2007 *ACM Computing Frontiers Conference*.
- General co-chair of 2008 *High-Performance Embedded Architecture and Compiler Conference* (HiPEAC).
- Organizer of the Barcelona Multicore Workshop held in Barcelona June 5-6, 2008
- Program vice-chair of Architecture Track of *2007 IEEE International Parallel and Distributed Processing Symposium*.
- Program co-chair of the *14th IEEE International Symposium on High-Performance Computer Architecture* 2008.
- Program chair of the *2009 IEEE International Parallel and Distributed Processing Symposium*.
- Program vice-chair of the Computer Architecture and Real-Time Systems Track for the *2010 ACM/IEEE International Conference on Computer Systems and Applications*, Tunisia, May 2010.
- Program chair of *ACM International Conference on Supercomputing* (ICS), 2014.
- Program track chair, architecture, *SBAC-PAD* 2017

- Program co-chair of *IEEE/ACM PACT* 2018
- Program area chair – computer architecture – *IEEE International Parallel and Distributed Processing Symposium 2019* – Rio de Janeiro
- Industry Liaison Co-chair for ISCA 2018
- Program co-chair of *APPT 2019* in Tianjin, China
- Organized Multicore Day in Stockholm 2018
- Organized HiPEAC spring Computing Systems Week in 2018
- Organizer and co-founder of the MULTIPROG Workshop in response to the programmability challenges of the multicore trend held in conjunction with the HiPEAC conference series (2007-2015): First edition on January 27, 2008 in Göteborg, in Paphos Cyprus in 2009 for the second time, in Pisa, Italy in 2010 for the third time, in Heraklion, Greece in 2011 for the fourth time, in Paris in 2012 for the fifth time, then in Berlin 2013, Vienna 2014 and Amsterdam 2015.

ACM and IEEE Committee Service

Summary: I have an unusually long service record. I am most proud of having been the first European in the committee of the prestigious ACM Turing Award.

- ACM SIGARCH Alan Berenbaum Distinguished Service Award Committee (2024-2026), Chair 2025.
- IEEE Fellow Committee, 2012 – 2015, 2017, 2018 and 2021
- ACM SIGARCH/SIGMICRO CARES member 2021-2025, Co-chair since 2022.
- ACM SIGARCH CACM research highlights committee to nominate the articles to be highlighted from the top venues in Computer Architecture: 2019, 2020 and 2022.
- Member-at-Large (2014-2018) in ACM Council, 2014 – 2018
- Member of ACM Europe Council, 2015 – 2017
- Member of Heidelberg Laureates Forum committee, representing ACM, 2013 – 2018
- Member of ACM Turing Award Committee (The “Nobel Prize” Committee of Computing Sciences), 2013-2018.
- Member of the ACM SIGARCH Maurice Wilkes Award Committee 2014-2016 (Chairman 2015)
- Member of the ACM SIGARCH Maurice Wilkes Award Committee 2017 (Chairman) due to a conflict-of-interest situation.

- Member of the IEEE/ACM Eckert-Mauchly Award Committee 2014-2017 representing ACM and Chairman in 2015.
- Member of the IEEE/ACM Eckert-Mauchly Award Committee 2019-2021 representing IEEE CS and Chairman in 2021.
- Member of IEEE TCCA Award Committee for the Young Investigator Award 2019-2021 (Chairman in 2020).
- Member of IEEE TCCA Member-at large 2020 - 2024
- Re-elected as Member of the IEEE TCCA since 2023
- On the Steering Committee of ACM International Conference on Supercomputing, 2014 – 2017
- On the Steering Committee of IEEE/ACM PACT, since 2018
- Member of the advisory committee of IEEE CS TCCA (2001-2005)
- Member of the Steering Committee of IEEE/ACM 28th, 29th, 31st, 32nd, and 33rd ISCA
- Member of the Steering Committee of IEEE HPCA 2009
- Member of the Steering Committee of IEEE IPDPS 2009 and 2010
- On the IEEE Computer Society Publications Board (at large) 2012
- Member of the Steering Committee of ACM/SIGPLAN LCTES (Languages, Tools & Compilers for Embedded Systems) 2002 - 2006.
- Member of the Steering Committee of the Int. Conf. on High-Performance and Embedded Architectures and Compilation (HiPEAC) (since 2005).
- Member of the ACM SIGARCH Distinguished Service Award Committee 2008-2010 and Chairman in 2010.
- Member of Executive Committtee of IEEE TCCA 2011-2016.
- Member of the Executive Committee of IEEE TCCA, 2017-2018
- Member of TCCA Award Committee for the John Cocke Young Investigator Award 2011-2012 (Chairman in 2011).
- On the Board of Governors of ACM SIGARCH 2011-2013
- On the IEEE Computer Society Publications Board (at large) 2012
- Member of the IEEE TCCA Chair Nomination Committee 2001.
- Chairman of search committee for EiC for ACM TACO, 2019
- Best paper award committee for IEEE HPCA, 2020 and 2024
- Session chair of best paper award session and on the committee IEEE/ACM ISCA 2022

Other Committee Services

- Advisory committee for 2025 International Conference on Adcanced Parallel Processing Technology (APPT)
- Member of European PRACE scientific committee, 2016 - 2018
- On the steering committee of the HiPEAC Conference since the beginning in 2005. Since 2008 Steering Committee Chair. Together with Koen De Bosschere we

reformed the conference and its publication model in 2012. The Paris venue attracted around 400 participants and the attendance has been growing since then.

- Co-founder of the Swedish Multicore Initiative and its Multicore Day organization from 2007 and onwards. Organizer of the 2010 Multicore Computing Workshop at Chalmers University of Technology.
- Member of the Advisory Board of the EUROPAR conference series, since 1995.
- Chairman of Steering Committee for the International Conference on High-Performance and Embedded Architectures and Compilers series. 2007 – 2012
- Member of the HiPEAC SC from its start 2004 until 2022
- Organized the 2012 HiPEAC Computing Systems Week April 2012.
- Member of the Swedish Research Council for Research Infrastructures, 2012 – 2014.

Panel Participation

- Moderator on a panel of the 3rd IEEE workshop on Scalable Shared-Memory Multiprocessors in San Diego, May 1993.
- Moderator on a panel on the 5th IEEE workshop on Scalable Shared-Memory Multiprocessors in Santa Margherita Ligure, Italy, 1995.
- Organized a task force on "Architectural Trends for Shared-Memory Multiprocessors" in conjunction with HICSS'97 Wailea, Hawaii.
- Panelist at the IEEE workshop CANPC'98 in conjunction with HPCA'98
- Panelist at the IEEE workshop CAECW'2000 in conjunction with HPCA'2000
- Organized a panel at the Sixth Swedish Workshop on Computer Systems Architecture, Gothenburg, May 1998.
- Organized a panel at IPDPS 2007 on Multi-core issues.
- Organized a panel at IPDPS 2011 on the Future of Computing

Services to National Bodies and Chalmers

- Expert in the procurement committee of a supercomputer platform at Chalmers to service computational scientific problems in virtually all disciplines at Chalmers (1996-1997)
- Participated in the development of D++, a new education program in Computer Science and Engineering. Specifically, I designed a specialization in Computer Systems (1995-1999).
- Chair of the council for the faculty of the School of Electrical Engineering and Computer Science (1998-1999).
- Member of working group to review Forskning 2000, a governmental evaluation of the research policy for the next decade (1999).
- Vice-dean of the School of Electrical and Computer Engineering with responsibility of the Ph. D. Education between 1999-2002.
- Vice-dean of the School of Computer Science and Engineering with responsibility of the Ph. D. Education between 2002-2003.
- Member of the Faculty council between 1999 and 2002.

- Member of working group to provide the government with input for strategic research actions, Dec 1999.
- Member of the recruitment committee at the School of EEC and M&CS from May 2000 and Jan 2001, resp. until 2002. Between 2002 until 2005, I held the same position in the school of CSE.
- Chair of the faculty search committee at the IT University of Goteborg between 2002-2005 and continued to serve this committee until 2007.
- Chair of the research committee at the School of Electrical and Computer Engineering, from June 2000 until 2002.
- Member of the steering committee for the planning of the IT-University in Goteborg between 2000 and until a permanent organization was formed in 2002.
- Member of the admission committee for selecting 3rd-grade students at the engineering programs for studies at foreign partnership universities (2001-2003)
- Member of the steering committee for student recruitment strategies at Chalmers, 2001-2002.
- Chair of the departmental recruitment group to be responsible for the process of recruiting (non-tenured) assistant professors to the department and to provide recommendations on promotion cases to the department head. 2010-2012.
- Member of Committee at the IT-University to look at the interaction between IT and the different area of advances in 2011.
- Member of committee to evaluate the applicants for Knut and Wallenberg Fellow to be submitted by Chalmers in early 2012.
- Member of search committee to recruit a new chairman of the computer science and engineering department in the spring of 2012.
- Member of the faculty search committee for the IT faculty of Gothenburg University. 2012-
- Co-chair (with Prof. Aarne Ranta) of the faculty council (to consolidate the view of faculty members) at the Department of CSE, 2013-2015.
- Member of search committee to recruit a new chairman of the computer science and engineering department in the spring of 2014.
- Division head of Computer Engineering, April 2015 – 2023
- Member of reference group of Research evaluation, (Affe Almgren) 2017

Program Committees

- **Summary:** I have serviced as member of program committees about 90 times.
- ACM/IEEE International Symposium on Computer Architecture (ISCA): 1996, 1997, 2000, 2003, 2004 (chair), 2006, 2010, 2011, 2012, 2021, 2022. ERC 2015, ERC 2016, ERC 2017, ERC 2019, ERC 2020. ERC 2024.
- IEEE International Symposium on High-Performance Computer Architecture (HPCA); 1996, 1997, 2000, 2001, 2002, 2006, 2008 (program co-chair), 2011, 2012, 2013, 2014 (Proxy PC chair), 2016 (proxy PC chair), 2019, 2017 (ERC) 2018 (ERC), 2020, 2021, 2022 (ERC), 2023.

- ACM/IEEE Micro: 2004 and 2005. SIGARCH and TCCA. On the ERC 2012, 2015, 2016, 2021, 2022. ERC 2024.
- IEEE IPDPS: 2003, 2004 (vice-chair), 2006, 2007 (vice-chair), 2009 (program chair), 2019 (vice chair), 2020 (vice track chair), 2022
- IEEE Top-pick issue in IEEE Micro Magazine, 2012.
- IEEE Top-pick issue in IEEE Micro Magazine, 2018
- Member of the program committee of the Branch Prediction Competition ISCA 2016
- IEEE ISPASS 2005 and 2006
- IEEE ICDCS 1992 and 1993 (vice-chair)
- IEEE PACT 2004, 2007, 2009, 2013, 2014, 2017, 2018 (co PC-chair), 2020
- EEE SPDP 1996
- ACM ASPLOS 1996, 2000, 2006, 2012. On review board 2010, 2023 (ERC)
- ACM SC 1997
- ACM ICS 1998, 2003, 2004, 2005, 2014 (program chair), 2017, 2020
- ACM HiPC 2003, 2004 (vice-chair), 2005.
- ACM LCTES 2003 (program chair), 2006.
- ACM Computing Frontiers 2005, 2007 (program co-chair)
- EuroPar 2 1995, 1997 (chair for topic), 1999 (vice-chair for topic), 2000 (chair for topic)
- PDCS 1997, 1998, 1999
- HIPEAC 2005, 2007 (program co-chair), 2009.
- DATE 2006, 2007
- SSS 2009
- SBAC-PAD 2011, 2016, 2017 (track chair)
- ICPP 2022
- MPP 2018
- **Workshops:** CANPC'97 and CANPC'98, EWOMP'99, IEEE Memory Wall workshop (in conjunction with ISCA 2000), MEDEA workshop in conjunction with PACT 2000, 2006, 2007, and 2009. EASY workshop in conjunction with ISCA-2001. MTEAC-6 in conj. with MICRO-35, 2002. dasCMP 2005, dasCMP 2006, dasCMP 2007, dasCMP 2008. MULTIPROG 2008, 2009 and 2010 (in conj. with HiPEAC) as organizer, WRC 2008 and 2009 (in conj. with HiPEAC), WIOSCA'2010 (in conj. with ACM/IEEE ISCA), BMW 2008, 2010.

Scientific Evaluation Assignments

Summary: I have a long track record of service doing evaluations of scientific projects and individuals applying for faculty positions. I am most proud of having acted as Chair of the Computer Science Panel Vetenskapsrådet and as panelist in the Computer Science Panel of the European Research Council (ERC).

- Review of research grant proposals for the National Science Foundation (NSF) (1991,1997), the Swedish Research Council for Engineering Science (TFR) (1995), the Swedish Foundation for Strategic Research (1998-1999), and the Norwegian Science Foundation (NFR) (1996-2000),
- Chair of evaluation panel in CS for the Swedish Research Council (Vetenskapsrådet in Swedish) 2001-2004.
- On the evaluation panel of the priority program on Organic Computing for the German Science Council (DFG), February 2005
- On the panel to evaluate prolongation of research programs in CS for SSF, December-January 2005/2006.
- Member of the Swedish Research Council for Research Infrastructure 2012-2015
- On the panel of Swedish Foundation of Research in the program of Future Research Leaders, 2019
- Elector of Vetenskapsrådet 2015, 2018, 2021 (nomination committee).
- Expert evaluations of applications for associate professorships in computer science and engineering at Kristianstad University College (1993), Lund University (1994), Karlskrona/Ronneby University (1995,1999), Chalmers University of Technology (1994, 1997), Royal Institute of Technology (1997, 1998, 2000), Luleå University (1998, 2000), Kuwait University (1998), Uppsala University (1999, 2002), Trollhättan (2003). Mälardalen (docent) 2005, 2008, University of Cyprus (2006, 2012), Linné universitetet Växjö (2012, 2013 – research portfolios for internal funding), Högskolan Väst (2013 - docent), Uppsala University (2014 – docent).
- Evaluations for promotion to assistant/associate professor (U.S.A.): Rice university (1998), Cornell University (1998), Princeton University (1999), Rochester Univ. (2001), Rutgers University (2002, 2003), University of Maryland (2003). University of Illinois - Urbana Champaign. (2004), University of Massachusetts, Amherst (2005), Harvard (2009), Penn State (2010), University of Cyprus (2007, 2012) Carnegie Mellon University (2012), North Carolina State University (2012), University of Michigan (2012).
- Evaluations for promotion to Reader at Imperial College (U.K.) (2001), Full professor promotion University of Edinburgh (2005), Reader, Edinburgh (2009), Full professor promotion University of Edinburgh (2012), Technion (2016).
- Evaluations for promotion to full professor (U.S.A & Canada): University of Minnesota (1999), Georgia Institute of Technology (1999), Rice University (1999), University of Texas at Austin (2000), University of Southern California (2003), University of California, San Diego (2003), Northeastern University (2004),

Rochester (2006), CMU (2006), University of Colorado (2008), North Carolina State University (2011), University of Toronto (2012), Princeton University (2012), UC Riverside (2012), UC Santa Barbara (2013), Duke (2014), Rochester (2016), Stanford (2017), Georgia Tech (2017) MIT (2022)

- Expert evaluations of applicants for full professorships at Luleå Technical University (1996, 2004), the University of Mälardalen (1997,1998,2001), Karlskrona/Ronneby University (1998), Uppsala (1999), Royal Institute of Technology (2000,2003), and Jönköping University (2002), Denmark Technical University (2005) TU Vienna (2015), Uppsala (2017), Royal Institute of Technology (2019), Linkoping (2020), KTH (2021)
- Member of a group to establish criteria for applications for promotions to full professors at Uppsala University and Umeå University (1999).
- Member of the National Committee for promotion to full professor in Computer Science (1999)
- Reviewer and member of evaluation committees of Ph. D. theses at Royal Institute of Technology (1992, 1997, 1998, 2004, 2015, 2020), Uppsala University (1994,1997,2000, 2002, 2006 x3, 2016, 2019, 2020), Chalmers University of Technology (1994,1998,2001,2006), Oslo University (1998), Joensuu University, Finland (1998), University of Paris Sud (2002,2005), Luleå University of Technology (2000, 2004). IT-university, Göteborg (2004, 2006), Blekinge Institute of Technology (2005, 2014), TU Delft (2006,2011), University of Edinburgh (2008), Murcia (2009), UPC (2010), Vaxjo (2010), DTU (2011), Murcia (2012), EPFL (2013), University of Illinois, UC (2013), FORTH and University of Crete (2013), Ghent University (2014) University of Amsterdam (2015), Tromsö (2019), Lund (2019), Lund (2023), Trondheim – opponent – (2024), Lund (2024).
- Jury member at Dr. Pascal Sainrat's habilitation dissertation at University of Paul Sabbatier and Institute de Recherche en Informatique de Toulouse, March 1998.
- Jury member and referee of Stephane Louise's Ph. D. thesis at University of Paris Sud. Jan 2002.
- Jury Member of the Ph.D. dissertation of Christian Fench (Edinburgh, 2008).
- Jury Member of Ph. D. dissertation (Manchester 2009).
- Faculty opponent at Knut Omang's thesis defense at University of Oslo in June 1998.
- Faculty opponent at Uppsala University, May 25, 2000, for Mikael Sjödin.
- Faculty opponent at Uppsala University, April 2016.
- Faculty opponent at Liv Vran's thesis defense at the Arctic University, Tromsö, Feb 15, 2019.
- Member of a committee to define the scope of a new EU-IST program on "Emerging Computing Architectures: New Processor Architectures and Advanced Compiler Technologies" in the spring of 2004.
- Recipient of a certificate of belonging to the category of best senior reviewers for IEEE Computer in 1994.
- PhD Jury member INRIA/University Paris Sud Daniel Gracia Perez, October 2005.
- Reviewer for Vaxjo University for research proposals. Oct 2010, 2013, 2015.

- Expert evaluator for EU FP7 IP TeraFlux for the European Commision, 2011, 2012, 2013 and 2014.
- Expert evaluator for ERC senior grants (2010, 2011, 2017)
- Reviewer of research proposals from Qatar National Research Fund (2011).
- On the European Research Panel for Computer Science "Consolidator grants", 2014, 2016, 2018 and 2020.
- On the evaluation panel of the Knowledge Foundation 2014 – 2021.
- Reviewer for ERC Synergistic grant proposals: 2019
- Reviewer for KAW proposals 2019.
- Referee for Research Fellows for the British Royal Society 2015 University Research Fellowship
- Habilitation jury member Stephane Louise, Paris 2015
- Patent litigation case for Wilmer Cutler Pickering Hale and Dorr LLP in 2015
- Evaluation of researchers at Linneaus University 2015
- Evaluation of research proposals for ERC and for Norska forskningsrådet 2017
- Evaluation of research proposals for Norska forskningsrådet 2019 (four)

Invited lectures

- **Summary:** I have been invited to give about 200 international lectures and among them 13 keynote addresses and talks at more than 40 universities and companies around the world.

- Carnegie-Mellon University, Pittsburgh, U.S, Oct. 1986.
- IBM Yorktown Heights, New York, U.S., Oct. 1986.
- PARLE conference, Eindhoven, Holland, June 1987.
- HICCS'21 A Cactus Stack Multiprocessor Memory Organization" HICSS'21 conference, Hawaii, U.S., Jan. 1988.
- N.E.C. Corporation, Kawasaki, Japan, Dec. 1988.
- International seminar on performance of distributed and parallel systems, Kyoto, Japan, Dec. 1988.
- 16th ISCA, Jerusalem, Israel, June 1989.
- Hebrew University, Jerusalem, Israel, Jan. 1990.
- University of Washington, Seattle, U.S., Sept. 1990.
- Ready Systems Inc., Sunnyvale, U.S., Sept. 1990.
- U. C. Berkeley, Berkeley, U.S., Sept. 1990.

- Stanford University, Stanford, U.S., Sept. 1990.
- International Computer Science Institute (ICSI), Berkeley, U.S., Sept. 1990.
- University of Southern California, Los Angeles, U.S., Sept. 1990.
- Dolphin Server Technology A/S, Oslo, Norway, Nov. 1990.
- Oslo University, Oslo, Norway, Nov. 1990.
- University of Edinburgh, Edinburgh, U.K., May 1991.
- Stanford University, Stanford, U.S., June 1991.
- Intel Corporation, Santa Clara, U.S., Dec. 1991.
- 20th International Conference on Parallel Processing, Chicago, 1991.
- University of Southern California, Los Angeles, U.S., Dec. 1991.
- International Parallel Processing Symposium, Los Angeles, U.S., March 1992.
- 19th ISCA, Gold Coast, Australia, May 1992.
- Stanford University, Stanford, U.S., Jan. 1993.
- M.I.T., Cambridge, U.S., Jan. 1993.
- New York University, New York, U.S., Jan. 1993.
- ICSEE'93 conference, San Diego, Jan. 1993.
- University of Southern California, Los Angeles, U.S., Jan. 1993.
- 3rd Workshop on Scalable Shared-Memory Multiprocessors, San Diego, U.S., May 1993. Moderator on a panel.
- University of Michigan, Ann Arbor, U.S., April 1994.
- 4th Workshop on Scalable Shared-Memory Multiprocessors, Chicago, U.S., May 1994.
- G.M.D., Berlin, Germany, June 1994.
- Ecole d'ete des jeunes chercheurs (summer school), Toulouse, France, July 1994. (Invited)
- University of Southern California, Los Angeles, U.S., January 1995.
- Stanford University, Stanford, U.S., January 1995.
- Tech talk at Sun Microsystems, Menlo Park, U.S., January 1995. (Invited)

- 5th Workshop on Scalable Shared-Memory Multiprocessors, Santa Margherita Ligure, Italy, June 1995.
- University of Washington, Seattle, U.S, Sept. 1995 (Colloquium, invited)
- University of Southern California, L.A., U.S, Sept 1995
- Digital Equipment Corporation WRL, Palo Alto, U.S. Sept 1995.
- University of Pisa, Feb. 1996.
- Hawaii International Conference on System Sciences, Wailea, Maui, Jan. 1997
- Gave a tutorial at EUROPAR'97, Aug. 1997, in Passau, Germany (Invited)
- Invited talk at EUROPAR'97, Aug. 1997 in Passau, Germany
- Invited talk at INFOFEST'97 in Montenegro, Jugoslavia, Sept. 1997.
- Panelist at CANPC'98 in conjunction with HPCA'98, Las Vegas, Feb. 1998 (Invited).
- Gave a tutorial at Technical University of Catalunya, Barcelona, Spain, Feb 1998. (invited)
- Universitet Paul Sabatier (and IRIT), Toulouse, France, March 1998.
- Ericsson Research, Älvsjö, April 1998.
- 1998 IEEE Workshop on Computer Architecture Education in conjunction with 25th ISCA in Barcelona, June 1998. (Invited)
- ARTES Summer school, Lidingö Stockholm, Aug. 1998. (invited)
- Sun Microsystems, Menlo Park, CA, Sept. 1998.
- Research overview at the Winter Meeting for CS Dept., Chalmers, Smögen, Jan 1999
- Thread-Level Data Speculation Techniques, Ericsson Research, Älvsjö, April 12, 1999
- All-Software Thread-Level Data Speculation Systems, Dagstuhl Seminars, April 21, 1999 (Invited)
- Polytechnic University of Barcelona, "On the Interaction between Commerical Workloads and Memory Systems in High-Performance Servers," Sept 9, 1999.
- University of Maryland, "On the Interaction between Commerical Workloads and Memory Systems in High-Performance Servers," Colloquim, Invited talk, Sept 16 1999.
- University of Southern California, "On the Interaction between Commerical Workloads and Memory Systems in High-Performance Servers," Sept 20, 1999.

- Princeton University, “On the Interaction between Commerical Workloads and Memory Systems in High-Performance Servers,” Sept 22, 1999.

- Panelist at CAECW at HPCA-6 in Toulouse, January 9, 2000.

- ETH, Switzerland, Colloquium, June 8, 2000 “Access Latency Reduction and Hiding Techniques for High-Performance Computers”. (Invited)

- ETH, Switzerland, June 9, 2000 “Boosting Energy-Efficiency for Off-Chip Caches using Small Block Sizes and Selective Prefetching”.

- Imsys AB, Stockholm, Aug 7, 2000 “Challenges in Computer Architecture”

- “Understanding Performance Bottlenecks in Complex Computer Systems” (invited talk), First Summer school on Engineering of Complex Computer Systems, Skövde University, Aug. 15., 2000.

- Metoder för effektivt utnyttjande av multiprocessorteknologi i transaktionsorienterade system: Project presentation at the NUTEK program conference, Lund, Sept. 11, 2000.

- Opening address at IEEE/ACM Int Symp. on Computer Architecture (ISCA-2001) July 2, 2001 in Gothenburg.

- “Can We ever Dream of Making Multiple Processors and Caches Appear as a Simple and Single Entity to the Software” Keynote speech at ICPP-01 on Sept 7, 2001. Valencia, Spain. (Invited)

- “All-Software Thread-Level Data Speculation on Multiprocessors” Invited talk at University of Paris-Sud XI, Jan 21, 2002.

- Lecture series in Parallel Computer Architecture. Technical University of Catalonia, Barcelona. April 2002. (Invited)

- Keynote Talk at IPDPS-2003 (Invited)

- Distinguished Lecture Talk at University of Southern California, January, 2003 (Invited)

- Several talks at Sun Microsystems during spring 2003 during my sabbatical there.

- Colloquium at University of Texas, Austin, April 7, 2003. (Invited)

- NSF Panel, June 2003 (Invited).

- IT-University, Göteborg, Sept and Oct 2003

- Lund University, Nov. 2003

- Keynote speech at ACM HiPC’2003 in Hyderabad (India), December 20, 2003 (Invited)

- Sun Microsystems, Feb 9, 2004

- Computing Frontier conference, Ischia, Italy, April 15, 2004 (Invited)

- Opening Address at 31st International Symp. on Computer Architecture, Munich, June 2004.
- Sun Microsystems, August 9, 2004
- "A Robust Memory Compression Scheme" (Invited) University of Illinois Urbana-Champaign, December 2004.
- ACACES 2005. Summer school arranged by HiPEAC on Chip-multiprocessors. July 2005, Italy. (Invited)
- Sun Microsystems, Nov 2, 2005.
- Keynote speech at the First HiPEAC conference, Barcelona, Nov. 18, 2005. (Invited)
- Keynote speech at 12th IEEE Symposium on High-Performance Computer Architecture, Feb 14, 2006, Austin Texas.
- Sun Microsystems, Feb 16, 2006.
- Multi-core Expo, Munich, Nov 16-17, 2006, invited talk
- EU FP7 conference, invited talk at session on Computing Systems, Nov 21-22, 2006, Helsinki
- Moderated a panel on Multi-core challenges at IPDPS 2007.
- Invited talk at DATE on future of computer architecture, April 17, 2007.
- Invited talk at Google, Trondheim, Norway, May 3, 2007
- Invited talk at Ericsson AB, May 24, 2007
- Invited talk at BSC/UPC Barcelona, July 31, 2007
- Invited talk at Stamatis Vassiliadis Symposium, Delft, Sept 28, 2007
- Talk at FET ICT Consultation workshop on "Massive ICT Systems", Brussels, November 7, 2007.
- Talk at EU IST FP7 Consultation workshop on "High-Performance Computing Systems", Brussels, Dec 17, 2007.
- Invited talk at University of Edinburgh, May 12, 2008.
- Invited talk at the Barcelona Multicore Workshop, June 5, 2008
- Panelist on a panel arranged by Yale Patt at the Barcelona Multicore Workshop, June 5, 2008
- HiPEAC presentation at EU meeting in Seoul Korea, June 16, 2008 (invited)
- Keynote presentation at ISCA workshop, June 21, 2008, Beijing, China.(invited)

- Presentation at Multicore Days Stockholm September 11-12, 2008
- Panelist at Multicore Days, Stockholm Sept. 11-12, 2008
- Talk in Lund on October 17.2008
- Presentation at “Multicores: Theory and Practice” in the EU project ACTORS at Technical University of Kaiserslautern, Germany October 28, 2008
- Panelist at the SMART 2009 workshop held in conj. with 4th Int. Conf on HiPEAC, Cyprus 2009.
- Panelist at the 2009 International Parallel & Distributed Processing Symposium.
- Gave a talk at Multicore Day in Kista on September 15, 2009 on how to use Nema Labs technolgy to make the code multicore ready.
- Gave a talk at PACT 2009 on our work on Zero-Value Caches. Sept. 2009
- Gave a talk at SC 2009 on the FASThread technology. Nov 2009
- Gave a talk at University of Washington on the FASThread technology. Nov 2009
- Gave a course on business idea identification at ACACES HIPEAC Summer school, July, 2010
- Participated on a panel at SAMOS 2010, July 19-22, 2010.
- Gave a talk at the ICT2010 European IST event in Brussels Sept 28, 2010.
- Panel at BMW Barcelona, Oct 21., 2010. Moderator: Avi Mendelson, Microsoft.
- Panelist at Workshop on Computer Architecture Education in conjunction with 2011 HPCA.
- Föreläsning på Rotary i Göteborg “Mikroprocessorn: Maximal Drivkraft i Minimalt Format” 7 februari, 2011.
- Invited talk at University of Texas at Austin “Scalability Challenges for Future Chip Multiprocessor Architectures” February 17, 2011
- Keynote at 2011 International Conference on Architectures of Computing Systems. Feb 24, 2011
- Invited talk at the 2011 Spring Industrial HiPEAC Workshop on Research in Academia and Industry: Insights from Nema Labs. April 6, 2011.
- Popular lecture at Vetenskapsfestivalen 2011.
- Moderator for “Looking Ahead” Panel at 25th IPDPS. May 2011 Anchorage.
- Invited talk at Multicore Day in Stockholm (Sept 15, 2011): Scheme: Software Abstractions for Heterogeneous Multicore Systems.

- Organizer of the EuReCCA workshop in Barcelona on November 4, 2011
- Organizer of the HiPEAC Spring Computing Systems Week in Göteborg, April 2012
- Invited talk at MATEO 2012. June 29, 2012.
- Invited talk at USC, November 2012.
- Invited talk at Workshop on Transfer to Industry and Startup (TISU) in conjunction with 9th HiPEAC. January 2013.
- Invited talk, University of Delaware, May 10, 2013
- Keynote at Gompute in Göteborg, 2013 (invited), April
- Keynote at PACT, Edinburgh (invited), 2013, September.
- Keynote APPT Conference (invited), 2013, August.
- Invited talk Multicore Day September 2013.
- Talk at Google on Cache Compression. (20 December 2013).
- Invited talk for DATE 2014 Hot Topic Session on Dark Silicon, March 27, 2014
- Invited talk at UIUC May 12, 2014 (host: Josep Torrellas)
- Invited talk at Ghent University May 27, 2014 (host: Lieven Eeckhout)
- Invited talk at FORTH, Crete July 10, 2014 (host: Manolis Katevenis)
- Invited talk at University of Texas at Austin (Yale-75), September 19, 2014
- Invited talk at ICT, Academy of Science, Beijing, China, Oct 9, 2014
- Invited talk at IBM Research, Beijing, China, Oct 10, 2014
- Invited talk at Beihang University, Beijing, China, Oct 12, 2014
- Invited talk at Xi'an Jiaotong University, Xi'an, China, Oct 15, 2014
- Blaze memory. Presentation at the Euroserver workshop in conj. w. HiPEAC, Jan 20, 2015
- Talk at Stanford University March 23, 2015
- Talk at Google, March 23 2015
- Talk at Qualcomm in San Diego, March 24, 2015
- Talk at AMD in Santa Clara, March 25, 2015
- Talk at NVIDIA, March 26, 2015

- Talk at Oracle, March 26, 2015
- Vetenskapsfinalen 2015 “Snabba och gröna datorer”, April 19, 2015
- Keynote at HiPEAC CSW in Oslo, May 6, 2015
- Zeropoint Memory Systems, technical talk at Facebook, Menlo Park, CA, June 23, 2015
- Zeropoint Memory Systems, technical talk at Samsung, Mountain View, CA, June 24, 2015
- Invited talk at the MULTIPROG workshop in conjunction with HiPEAC 2016, Jan 18 2016
- Invited talk at the “MICROSERVER: Energy-efficient microservers” workshop in conjunction with HiPEAC 2016, Jan 20, 2016
- Invited talk at ROMOL 2016 in conjunction with HPCA 2016
- Talk at HPC Summit May 10, 2016
- Invited talk at the NSF workshop WASEA on future research trends for compilers and architecture in conjunction with PACT, September 2016.
- Talk at HPC Summit in Barcelona, May 2017.
- Talk at Huawei, June 2017
- Summer school class at UPMARC June 2017
- Samos July 2017
- Panel speaker at the ACM Conference, September, 2017
- Talk at ACM Conference on EuroLab-4-HPC, 2017
- Talk at Rio University, October, Brazil, 2017
- Panel speaker at SBAC-PAD 2017 in Campinas, Brazil. Oct. 2017
- Keynote speaker at MCC, Uppsala, December 2017
- Energiseminarium. SO Energi. IKT är en energislukare. 14 december, 2017
- Keynote talk at the 17th International Symposium on Parallel and Distributed Computing, Geneva from 25th to 27th of June, 2018.
- ROMOL Invited talk Barcelona, March 2, 2018
- HPC Summit 2018
- Invited talk at Multicore Day, Nov 26 2018.

- Invited talk at Technion, November 2018
- Invited talk at Intel, Haifa, November 2018
- Invited talk at DATE 2019
- Invited talk at HiPEAC CSW spring edition in Edinburg 2019 (Parallelism management)
- Invited talk at HiPEAC CSW spring edition in Edinburg 2019 (Innovation)
- Invited talk at SIAT institute, Chinese Academy of Science, May 2019
- Invited talk RISC V Conference, June 2019.
- Invited talk at Yale anniversary in Barcelona July 2, 2019
- ACM summer school, July 2019, lecturer
- UC Berkeley September 2019
- Talk at WASP4ALL, November 2019.
- Virtual talk (via zoom) at University of Heidelberg, June 2020
- On the MICRO 2021 panel on "Microarchitecture research: The view from the Globe". Sept 2021.
- Invited talk at DATE 2022 on technology transfer. March 2022
- On the panel of 4th Undergrad Architecture Mentoring Workshop (uArch) at ISCA 2022
- ACM summer school, September 2022, lecturer
- Keynote address, December 2022, ACM HiPC, Bangalore
- Invited talk at IIS in Bangalore, December 22.
- Invited talk in the Distinguished Speaker program at Shanghai Jiao Tong University, December 2022
- Invited talk at the DAC Supercomputing Center in Bangalore, December 2022
- ACM summer school, July 2023
- Keynote speech at the 2023 China Computer Federation Systems Conference, August 5, 2023.
- Distinguished talk at University of Illinois, Urbana-Champaign, Oct 30, 2024
- Distinguished talk at University of Texas at Austin, Nov 7, 2024
- Invited talk at Norwegian Technical and Science University (NTNU), April 2025.

Research Grants

Summary: Over the years, I have received over 20 MEuro to fund my research. I am most proud of having won a European Researc Council (ERC) advanced grant (2.3 MEuro).

- The first name corresponds to the P.I.
- Lars Philipson and Per Stenström: *Laboratory of Experimental Computer Architecture*, 1990-1993, STU, about 2.4 MSEK
- Lars Philipson and Per Stenström*: Laboratory of Experimental Computer Architecture*, 1993-1996, NUTEK, about 1.8 MSEK.
- Per Stenström: *Scheduling of Memory Instructions for Shared-Memory Programs*, 1994-1997, TFR, about 1 MSEK
- Per Stenström and Per Andersson: *ATM-based Multiprocessor Interconnects*, 1994-1996, NUTEK, about 800 KSEK.
- Per Stenström: *Performance Prediction Testbed for Mobile Packet Data Applications*, 1996-1997, NUTEK. about 700 KSEK
- Per Stenström: *Methodologies and techniques to estimate worst-case execution time*. 1997-2002. TFR, about 1.8 MSEK.
- Per Stenström, Bengt Nordström, and Mats Viberg: Equipment grant from FRN, about 3,5 MSEK, 1997-2000.
- Per Stenström: *A New Approach to Memory Hierarchy Management in Shared-Memory Multiprocessors*. TFR/SSF, about 1.5 MSEK, 1998-2001
- Per Stenström: Donation of an E4000 multiprocessor server from Sun Microsystems. About 1 MSEK
- Per Stenström. Collaborative Research on Multiprocessors for Database systems. CR with Sun Microsystems. $50,000 from Sun Microsystems. 1998-2000.
- Per Stenström, *Design Strategies for High-Performance Real-time Multimedia Applications on Shared-Memory Multiprocessors*, SSF, about 3 MSEK 1999-2003.
- Per Stenström: *A New Approach to Thread-level Data Speculation Execution Models*. TFR, about 1 MSEK, 1999-2001.
- Per Stenström, "*Metoder för effektivt utnyttjande av multiprocessorteknologi i transaktionsorienterade system*, NUTEK about 700 KSEK, 2000.
- Per Stenström and Anders Ardö "*Networked implementation of a distributed electronic journal collection and full text archive*, NORDUNET-II, about 1 MSEK 2000-2001.
- Per Stenström (PI): "*Techniques for Module-Level Speculative Parallelization on Shared-Memory Multiprocessors*, SSF, 720 KSEK, 2000-2001

- Per Stenström (primary PI, together with Dr. Fredrik Dahlgren, Ericsson), *Support for Real-Time 3D Graphics for Future Mobile Terminals under Energy/Area Constraints*. SSF, 1.2 MSEK 2000-2004.
- Per Stenström and Michel Dubois: *MECCA: Meeting the Challenges in Computer Architecture*, collaboration grant 500 KSEK/year for 2001-2004 from STINT.
- Per Stenström. Methods for Adapting the Resource Demands in Computer Architectures under various Demand Objectives. Vetenskapsrådet, 1.8 MSEK, 2003-2006.
- Per Stenström (primary P.I.) FlexSoC: A Flexible Platform for System-on-Chip in Embedded Systems. SSF 10 MSEK, 2003-2007.
- Per Stenstrom (sole PI): Swedish Research Council 2004-2005. 1 MSEK.
- Per Stenström (Mateo Valero coordinator). *HiPEAC: High-Performance Embedded Architectures and Compilation Methods.*. EU Network of Excellence in Computer Architecture. 2004-2008. Leading a major effort as workpackage leader
- Per Stenstrom. *Compute Resources to Analyze Future Computer Architectures*. Admission to use the compute resources of SNIC.(2005-)
- Per Stenström (Stamatis Vassiliadis coordinator). *SARC: Scalable Computer Architecture*. EU Integrated project. 2006-2010. 6 MSEK. Leading a major effort as workpackage leader
- Per Stenström (Mateo Valero coordinator). VELOX - A STREP accepted by EU FP7. About 200 000 EU (2008-2010)
- Per Stenström (Koen De Bosschere coordinator). HiPEAC-2 Network of Excellence accepted by EU FP7. About 360 000 EU (2008 - 2012). Leading a major effort as workpackage leader
- Per Stenström (P.I.) Out-of-Order Thread Speculation. Swedish Research Council (2009 - 2012). 1.5 MSEK.
- Per Stenstrom, P.I. (and as co-PIs: Lars Svensson, Sally McKee, Per Larsson-Edefors) CHAMPP. Funded by the Swedish Research Councils with a budget of 3 MSEK (about 300,000 Euro) per year from 2010 - 2014.
- Industrial PhD (VR) 2010-2014
- Per Stenstrom P.I., Ericsson project 2010, 70 KSEK.
- Member of The EURO-TM COST action funded by the European Commission (2011-2014)
- Per Stenstrom, P.I. (and as co-PIs: Philippas Tsigas and Ulf Assarsson) SSF grant on software abstractions for heterogeneous multicores. 20 MSEK 2011-2016.
- Per Stenstrom, P.I. (together w/ Jan Jonsson as co-PI). Grant for a project with RUAG through NRFP. 1.2MSEK 2012-2014.
- Per Stenstrom (P.I.). Funded by the Swedish Research Council 2013-2017, 4.4 MSEK.
- Per Stenstrom and Georgi Gaydadjiev (P.I.). FP7 Project Euroserver 2013 - 2016 (about 6 MSEK)

- Per Stenstrom (P.I.) European Research Council (ERC) Advanced Grant. 2.3 M Euro (about 20 Million SEK) 2013-2018.
- ARTEMIS. EMC^2 (P.I. w/ Ioannis Sourdis) 2 MSEK
- Per Stenstrom (P.I.) ACE: Approximate Computing Systems. VR, 9 MSEK (2015-2019)
- Blaze Memory: Innovations kontoret Väst for interviews with end users, 2015 3 months, 60 KKR.
- Per Stenstrom (Coordinator) EuroLab-4-HPC. EC CSA FET 1.4 MEU. (2015-2017)
- VINN Verifiering for Blaze Memory, Vinnova, 400 KSEK for 4 months (2015)
- Autonomous systems and software development (David Sands P.I., Per Stenstrom and others co-P.Is.) 2015-2026. 1.8 BSEK.
- Per Stenström.TETRAMAX 2017. 1 MSEK
- Per Stenström. HIPEAC-5 2017. 0.5 MSEK
- Per Stenström. EUROLAB4HPC2 2018 1 MSEK
- Per Stenström. HiPEAC-6 2019 0.5 MSEK
- Per Stenström. EuroHPC 2020 “eProcessor” granted (15 MSEK over three years)
- Per Stenström. EuroHPC PILOT-1 (2021) granted (10 MSEK over three years)
- Per Stenström. EuroHPC and EPI2 (granted) 2021,10 MSEK
- Per Stenström. Swedish Research Council. PRIME. Konstruktionsprinciper för minnesberäknande parallella system. 2019-2023, 4MSEK
- Per Stenström. Foundation for Strategic Research. PRIDE. Principles for Computing Memory Devices. 28 MSEK
- Per Stenström. Wallenberg. SCALE-ML: Principles for Scalable Parallel Architectures for Machine Learning. 2020 – 2025 4 MSEK
- Per Stenström. Wallenberg Foundation. Research expedition Databound Computing. 2022-2027 4 MSEK
- Per Stenström. Wallenberg Foundation Twin-PhD project. Databound Computing. 2022-2027 4 MSEK
- Per Stenström. European Processor Initiative (SGA2). 2022-2025 10 MSEK per year
- Per Stenström. EU eProcessor. 2021-2025 10 MSEK per year
- Per Stenström. EU Pilot-1. 2021 – 2025 10 MSEK per year
- Per Stenström. EU HiPEAC 2021 – 2023 0.5 MSEK
- Per Stenström. SSF ClassIC 4 MSEK (PhD student at Lund University by courtesy)
- Per Stenström. EU DARE 2025-2030 10 MSEK per year
- Per Stenström. Vinnova Advanced Computing planning grant 0.2 MSEK (if granted)