CURRICULUM VITAE of Professor, Dr. Per Stenström

Fellow of the ACM, AAIA, and IEEE

Citation: ***"for contributions to design of high-performance memory systems"***

Member of The Royal Swedish Academy of Engineering Sciences,

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1. Academic Genealogy

Emanuel Björling (1839 – 1910) Professor of Mathematics, Lund University

Johannes Rydberg (1854 – 1919), Professor of Physics, Lund University – widely known for Rydberg's formula and constant.

Karl Manne Siegbahn (1886 – 1978), Professor of Physics, Lund University – Nobel Prize in Physics in 1924 for his discoveries in the field of X-ray Spectroscopy

Sten von Friesen (1907 – 1996), Professor of Physics, Lund University – known for his discoveries in Nuclear Physics.

Hellmuth Hertz (1920 – 1990), Professor of Electrical Measurement Technology, Lund University – known for his pioneering work on Inkjet and Ultrasound technology. His father got the Noble Prize in Physics in 1925 and his father's uncle, Heinrich Hertz, gave name to the unit Hertz for frequency.

Lars Philipson (1945 – 2008), Professor of Computer Engineering, Lund University – known for his pioneering work on multiprocessor technology and making VLSI design a Swedish academic subject.

Per Stenström (1957 –), Professor of Computer Architecture, Chalmers University of Technology, Alma Mater: Lund University – known for his pioneering contributions to the design of high-performance memory systems with innovations in cache coherency, latency tolerating techniques. memory and cache compression techniques and contributions to real-time systems, especially concerning the design of time-predicable computer architectures, a field he pioneered.

2. Experience

2.1 Current Activities:

Professor of Computer Engineering with a Chair in Computer Architecture, Chalmers University of Technology, Göteborg, Sweden since November 1995. My main current activities involve the following:

Management of a Research Program in Computer Architecture. The research focus is on design principles and design methods for embedded and high-performance computer systems. Research issues span memory system design, architecture support for parallel execution; transactional memory and thread-level speculation, resource management, performance analysis and modeling methodologies, real-time systems, and energy-aware system design tradeoffs. I recently concluded the ERC advanced Grant funded MECCA (Meeting the Challenges in Computer Architecture) project, an SSF founded framework program (Software Abstraction for Heterogeneous Multicore Systems), a VR funded framework program on Approximate Computing, coordination of EuroLab4HPC. Currently I represent Chalmers as a partner of the European Processor Initiative and related projects. I am the P.I. of the SSF funded PRIDE project started in 2021.

Teaching. I annually teach advanced courses in Computer Architecture. I released a textbook on Computer Architecture with Michel Dubois and Murali Annavaram: Parallel Computer Organization and Design, Cambridge University Press, in 2012. A new edition is underway and will be released in 2024.

Head of Computer Engineering Division. Since 2015 until 2023, I acted as the head with a head count of about 70 staff members (25 faculty members and 45 PhD students and postdocs.)

Professional service to the scientific community. I service, on a regular basis, program committees for top conferences in computer architecture. I chaired the prestigious IEEE/ACM Int. Symp. on Computer Architecture (ISCA) in 2004, IEEE HPCA in 2008, IEEE IPDPS in 2009, ACM ICS in 2014 and IEEE/ACM PACT in 2018. I was Associate Editor-in-Chief of Journal of Parallel and Distributed Processing (2010 – 2023), Senior Associate Editor of ACM TACO and Associate Editor and Topical Editor of IEEE TC. Previously, I have been an Associate Editor of IEEE Computer Architecture Letters 2001-2010, Subject Area Editor of Journal of Parallel and Distributed Computing 1993-2010, and Associate Editor of IEEE Trans. on Computers 2001-2004. I was the founding Editor-in-Chief of Transactions on HiPEAC, which was launched in 2006 until its termination in 2010, and I was an Associate Editor of IEEE Transactions on Parallel and Distributed Systems 2008-2010.

Entrepreneurship

I founded Nema Labs AB (founded in 2007) and was a member of its Board of directors. I was the CEO from 2007-2009. I take an active role in stimulating activities to bring research ideas to the commercial arena.

The Eurolab-4-HPC initiative was launched in 2015 and has gained lots of interest from the European Commission because of the pilot in acceleration of innovation instruments, called business prototyping.

In April 2015, I founded ZeroPoint Technologies AB together with my PhD graduate Angelos Arelakis with the mission of providing more memory capacity and memory bandwidth through an ultrafast and effective approach to compress and decompress memory data. I initially acted as the lead and then as chief scientist and president for ZeroPoint Technologies Inc. (incorporated in the state of Delaware, US)

Scientific advisory board. I was on the scientific advisory board of EASE, Lund University between 2010-2014.

Member of the board of Chalmers Innovation. I was on the Board of directors of Chalmers Innovation 2010 – 2015.

Other commisions

Member of the Swedish Research Council for Research Infrastructures, 2012 until 2014.

Member of the European Research Council panel on Computer Science, since 2014-2020.

Member of ACM Europe Council. I was a member of the Council from 2012 to 2016 and actively promote more European members to be nominated for advanced grades and having more conferences located to Europe among other tasks. I also served on the ACM Turing Award Committee from 2013 – 2018 to select the "Nobel Prize Winner" in Computing Science. I also offered my service on the Heidelberg Laurate Forum to select young researchers for the annual forum to meet with distinguished members of the Computer Science and Mathematics communities.

Member of the ACM Council. I was a member "at Large" to influence the policies of the ACM. Mandate period 2014-2018.

Awards committees. I have been on the ACM Turing awards committee, ACM/IEEE Eckert Mauchly awards committee, ACM Maurice Wilkes awards committee and IEEE Young Investigator awards committee.

2.1 Past Responsibilities:

Guest Professor of Göteborg University, 2002-2007

Deputy Dean of the IT University, 2002-2007

Both of these commitments had their roots in my active involvement in founding the IT-University in Goteborg. Early on, I was a member of the Steering Committee to establish the vision and strategic goals of an academic institution that should form an environment that promotes new disciplines in ICT that are of importance for the society through interdisciplinary cross-fertilization. The IT-University went from a project organization to a formal institution in 2002. I contributed to the developments by establishing a Bachelor and Master's program in Software Engineering together with Professor Lars Mathiassen. I also contributed operationally in processes to establish the agenda for the Ph. D. education and the recruitment plans and research funding strategies for this new academic institution. The software engineering platform is now one of the largest in Sweden.

Visiting Positions in the U.S.A.

I have had the privilege to work with so many wonderful and highly talented individuals in the past in a country that, in my view, is outstanding to leverage on individual assets, which has had tremendous impact on my views and my personal developments. The individuals I have been fortunate to collaborate with are listed explicitly below and deserve special mentioning. From a professional standpoint, they boosted my abilities to deliver high quality research and mentorship to young researchers and my understanding of how it can be best transferred to society in efficient ways.

- **Sun Microsystems** from December 2002 to July 2003. I did my sabbatical in the Advanced System Development Center and investigated concepts for future High-Performance Computer Systems. My manager there was vice-president Dr. Rick Lytel – a great role model in driving highly energetic teams. I continued as a consultant until 2006.
- **University of Southern California, Department of EE-Systems** from July 1993 to September 1993. I worked with Professor Michel Dubois on the specification of the architecture of an experimental shared-memory multiprocessor system. Michel and I have continuously worked together since 1990 – a great role model in science.
- **Stanford University, Computer Systems Laboratory** from June 1991 to December 1991. I worked with Professor Anoop Gupta on performance evaluation and architectural innovation of scalable shared-memory multiprocessor architectures. We developed the Flat-COMA proposal during that time. Anoop taught me a lot about high-quality research in computer architecture.
- **Carnegie-Mellon University, Department of Computer Science** from September 1987 to May 1988. I worked with Professor Zary Segall on implementation and evaluation of shared-memory models on distributed system architectures. We evaluated one of the first shared-memory model implementations on a distributed system.

In the really early phases of my career, I did the following

Associate Professor of Computer Engineering, Lund University, Sweden, from November 1993 until November 1995 (before that on the faculty since July 1988 and before that a Ph. D. student since February 1984).

- Taught graduate and undergraduate courses in Computer Architecture, Switching Theory, and Hardware Design and was director of studies between 1988-1995. I developed a textbook on basic computer organization and assembly language programming that was printed by Prentice Halls
- Led a research group between 1990 - 1995 in Parallel Computer Architecture. I supervised three Ph. D. students who successfully earned their degrees until my move to Chalmers. My group was very successful; we got five ISCA papers accepted during the five years this group existed before I left for a full professorship at Chalmers.
- Was member of the Board of the Graduate School of Electrical and Computer Engineering at Lund University since November 1993.
- Was acting full professor from January 1995 until June 1995.

Over the years I have been involved in the following activities paralleled with my chair in Computer Architecture at Chalmers:

Advisory Roles, Consultancy, and Commisions of Trust in Academia and Industry

Scientific advice. I was a scientific advisor of the Swedish Institute of Computer Science between 1995 and 1998 and acted as advisor for a handful PhD students.

Chair of the council for the faculty at the School of Electrical and Computer Engineering. Between July 1998 until I became a vice-dean in April 1999.

Vice-Dean of the School of Electrical and Computer Engineering. 1999-2001.

Vice-Dean of the School of Computer Science and Engineering at Chalmers. 2001-2003.

Member of the board of Blekinge Institute of Technology. 2001-2004.

Chair of the Research Evaluation Panel in Computer Science. I was the chair of the panel to evaluate research proposals sent to the Computer Science area in the Swedish Research Council between 2001 and 2005. My main role was to make sure that all applications are fairly evaluated by putting together a panel trusted by the community and by soliciting a large number of external reviewers. It was a very good learning experience in scientific leadership.

Board of Directors. Virtutech AB (1998 - 2002), I owned the technical perspective here in the board to understand what were the most strategic directions to take into the plan for company growth. Virtutech became a healthy startup and got headquartered in the US in 2002. In 2010, Intel acquired Virtutech. This mission sparked my interest in the big question how we can accelerate uptake of research ideas in the market place.

Technical advisor. Imsys AB (2001-2003) I helped this Swedish processor company to position itself in the market of microprocessors.

Consultancy. Sun Microsystems Inc. (2003-2006) I worked with Sun in capacity as an expert and was called in to take part in various design reviews. I also contributed with a lot of IP and filed eight patents of which seven have been approved.

Member of the Board of the IT University of Goteborg. 2006 - 2009.

Member of research priority panel for the Swedish Strategic Research Foundation (2006-2007) in the area of software. I pushed especially our need of a strategy towards multicore computers.

On the Council for Research Infrastructure (Swedish Research Council). 2012-2014

Member of the Board, Nema Labs AB (2007-2012)

Member of the Board, ZeroPoint Technologies AB, since 2015

President of ZeroPoint Technologies Inc., since 2017

Coordinator/PI or co-PI for ten major efforts:

PAMP (1998-2003) (Performance-demanding Applications on Multi-Processors) is a project funded by The Foundation for Strategic Research, which involves research groups at five research institutions and five companies across the country. The focus is on software and hardware design methods for using multiprocessors in industrial applications. The program ran for five years (from 1998-2003) with an annual budget of 5 MSEK and is sponsored by the Swedish Foundation for Strategic Research (SSF). The output of the number was truly amazing with about ten graduated PhDs.

FLEXSOC (2003-2007), The objective of this project was to build a heterogeneous SOC platform of a wide variety of core functionalities and make it significantly more programmable and energy-efficient. Our approach to make it more programmable was to define an architecture framework in which accelerators could be

added with a low performance and engineering cost. The output has been significant with a handful graduated PhDs and important results cutting across circuit techniques through computer architecture to compiler design. In the evaluation of the research program, it was noted that we had achieved significant results with limited funds.

CHAMMP (2010-2014). This project got funding in November 2009 from the Swedish Research Council. Its objective is to define new scalability paths for multicore chips to provide high performance across a large set of applications within the constraint of a limited power budget. Our approach is to explore adaptivity to processor cores as well as the memory system. It was overall a successful project that resulted in several interesting results on the topics of cache compression, energy-efficient cache design and hybrid memory technologies.

SCHEME - Software Abstractions for Heterogeneous Multicore Systems (2011-2016)**.** This project got funding in 2011 by SSF and its objective is to develop principles to design software modules that can abstract away architectural issues in parallel architectures to productivity programmers by designing software components that hide parallelism. It has generated several interesting results in the areas of transactional memory, lock-free data structures and in computer graphics.

MECCA – Meeting the Challenges of Computer Architecture. I earned in 2013 one of the most prestigious grants (ERC Advanced Grant) of 2.3 Million Euro to pursue a very ambitious research program to meet specific challenges in my field concerning management of Parallelism, Power and Predictability – the three Ps – in the context of future parallel computing systems.

ACE – Approximate Computing Systems. I earned in 2014 in tough competition a VR (Swedish Research Council) Framework program to study a new hardware/software interface for approximate computing in which the objective is to use algorithmic semantic information about numerical accuracy to build computers that can be substantially more power efficient.

EUROLAB-4-HPC. After four years of lobbying for a European virtual Center of Excellence in Computer Systems Technology, EC decided to form a call along aligned with this vision. My proposal was funded and the project started on September 1, 2015.

EPI …

PRIDE …

ClassIC…

Other Major Endeavors

Launch of a new publication model in computer engineering. Publishing in conferences is the preferred publication method in the field of computer engineering. This is not only inefficient but also hurts the discipline as bibliometric methods to count citations disfavor top-rated conferences. Together with Professor Koen De Bosschere and Tom Conte I convinced ACM TACO to try out a journal-first model in which we have encouraged submission of original research results in journals rather than in conferences

by a model in which accepted papers also are presented at a conference for dissemination. By forming an association between ACM TACO and the HiPEAC conference we have managed to increase the number of submissions to ACM TACO by a large factor. We have also shown that it is possible to cut down on the turn-around time for first response to two months making journal review processes as efficient as conference review processes.

Formation of the Eurolab-4-HPC pan-European Center on High-Performance Computing Systems. Together with Professors Mateo Valero (BSC) and Manolis Katevenis (FORTH) we have convinced the EC to fund a pan-European center in High-Performance Computing Systems. This center proposal is backed by top groups in computer architecture and by the leading companies in the domain.

1. Academic degrees

- **Docent degree in Electrical and Computer Engineering at Lund University**

November 1993.

- **Ph. D. degree in Computer Engineering**

  Thesis title: *Aspects of Memory Systems for MIMD Multiprocessors with a Shared-Memory Model*, Department of Computer Engineering, Lund University, May 1990. Thesis advisor: Prof. Lars Philipson

- **Master of Science in Electrical Engineering:**

  Thesis title: *Digital in- och uppspelning av deltamodulerat tal* (in Swedish),

  English: *Speech synthesis using delta modulation*

  Department of Computer Engineering, Lund University, October 1981.

  Thesis advisor: Prof. Lars Philipson

2. Research Focus

My whole research production has centered on the general question how to design general-purpose computer systems to deliver a high performance within the constraints of the technology and given current application and technology trends. In focusing on this general question, it has been important to me to take a holistic system view in addressing how applications, system software, and compiler technology interact with the hardware platform and how performance can be improved by design tradeoffs across the hardware/software boundary. My research has focused on improving multiprocessor technology primarily.

The key contributions I have made to the field of computer architecture concerns:

- *Shared-memory multiprocessor architecture*; specifically design of high-performance memory systems. I have made considerable contributions to the design of multiprocessor systems, especially how to make them scale to a large number of processors. I have been a key contributor to the general understanding of how to use caches in such systems to overcome the memory system bottleneck by a range of innovations regarding cache

coherence maintenance, latency tolerance techniques, and hardware/software tradeoffs in supporting memory consistency models. This work has been very influential. (IEEE and ACM Fellow citation "for his contributions to the design of high-performance memory systems)

- *Compiler optimization techniques;* specifically, to remove performance overhead associated with cache coherence maintenance. My early work, on using dataflow analysis techniques to reduce latency and bandwidth associated with loads and stores to shared data, has been quite pioneering. More recently, I have made considerable contributions to thread-level speculation and transactional memory which motivated me to launch a startup – Nema Labs in 2007.
- *Real-time aware architectures.* In real-time systems, it is important to guarantee that a computational task meet its deadline, i.e., one must establish the worst-case execution time (WCET) of a task. Unfortunately, WCET is often much longer than the actual execution time leading to gross over commitment of computational resources. With Thomas Lundqvist I contributed with a new approach to estimate WCET much more tightly than had been possible taking into account features of high-performance architectures such as caches and out-of-order execution. We also discovered that the conventional thought assuming a cache miss leads to the longest execution time is not true in out-of-order execution engines. The reason is that it can lead to timing anomalies which can yield incorrect WCETs. These works led to highly influential publications in IEEE RTSS, Journal of Real-time Systems and ACM TECS and have collected altogether close to a thousand citations.
- *Performance evaluation methodologies*; specifically simulation techniques based on direct execution and analytical models. I have contributed with improved methodologies for full system simulation by leading the developments of the CacheMire test bench and participated in the developments of Simics, a full system simulation platform. I've also developed analysis methods that can make accurate estimates of the worst-case execution time of programs on high-performance processors taking caching and multiple-issue pipelining techniques into consideration.
- *Thread-level speculative execution.* I've taken an interest in simplifying the task of extracting coarse-grained (or thread-level) parallelism out of sequential programs recognizing the possible trend of migrating multiprocessor support to the chip level. I've run several projects in which we consider hardware/software tradeoffs in the implementation of efficient speculation mechanisms and in how to extract module-level parallelism, i.e., parallelism across procedures, functions, and methods. This project has led to great insights on how to support this paradigm both at the hardware as well as the software level. It has been influential.
- A natural continuation of this work is on *transactional memory* which builds on cache coherence work I did in the past and my more recent focus on identifying useful support at the architectural level to ease parallel programming. My group has explored a wide range of hardware protocols for implementation of transactional memory with the goal of making them efficient and yet reasonably simple to implement to accelerate deployment in industry.
- *Design tradeoffs for high performance under power consumption constraints.* Another interest concerns how to do design tradeoffs to maximize the performance under energy dissipation constraints. My goal is to understand what affects architectural tradeoffs regarding high-performance memory system design and methodologies to aid designers in making such tradeoffs. In an early project with Ericsson Mobile Communication we especially considered architectural techniques to fuel the development of powerful handheld computers/phones. This project yielded many interesting results. We came up

with energy-efficient cache coherence solutions and helped define the key concept for snoop filtering which is widely used in machines today. We continued to look at techniques to improve utilization of memory resources.

- *Compression in the memory hierarchy.* During my sabbatical leave at Sun Microsystems in 2002/2003, I carried out a number of fundamental studies to quantify how well memory resources are used in cache hierarchies and in main memory. I made a number of observations that were going to steer some of my research over the next decade. One such observation is that data values stored in memory exhibit a high redundancy. I got interested in considering the prospect of compression to use memory resources more effectively first considering main memory (with Magnus Ekman), then the memory link to save memory bandwidth (with Martin Thuresson) and finally cache compression (with Angelos Arelakis). This led to a number of highly cited papers in ISCA 2005, IEEE Transactions on Computers, ISCA 2014 and in MICRO 2015 and the launch of a startup company (ZeroPoint Technologies).
- *Efficient computing.* My current thrust is to explore how we can achieve significantly higher compute efficiency by cross-cutting the transformation hierarchy. Especially, I am interested in leveraging obvious static information provided by programmers in modern task-based parallel programming models. Examples of obvious information is when tasks start/stop and what data they access. The run-time system can use this information together with dynamic information collected at the architecture level for resource management purposes. With Madhavan Manivannan, Miquel Pericas and Vassilis Papaeftstathiou, I have come up with cross-the-stack cache management. We have come up with cache management schemes that are far better in managing communication through new cache coherence optimizations and far better in detecting and eliminating dead blocks. Along the same theme, I am exploring how to build significantly more energy efficient systems by leveraging computational deadlines defined by programmers or system administrators and use those at the run-time system level to throttle computational resources. This is ongoing work with two PhD students (Mehrzad Nejat and Waqar Azhar), Miquel Pericas and Vassilis Papaefsthatiou. Finally, with Risat Pathan we have opened a new field of considering dynamic scheduling algorithms that can provide tight WCET guarantees for task-based parallel programs.

3. Teaching

My teaching experience ranges from developments of individual courses to specializations (suites of courses) in Computer Engineering. Apart from course developments, I have a strong interest in developing new pedagogical approaches to teach topics in complex engineering systems, especially using flipped class-room methods and blended learning approaches, i.e. MOOC technologies.

- I have taught courses on Digital Design, Computer Organization, Computer Architecture, and Parallel Computer Architecture over the past several decades.
- I've also been involved in curriculum design. In 1997 I led the development of an advanced program in computer systems within the computer science and engineering curriculum in computer systems engineering. The program is intended to provide an in-depth coverage of technologies and design methods for application-specific computer systems.
- I'm author of four textbooks on Computer Organization and Assembly Language Programming and Parallel Computer Organization and Design (see Section 5.1).
- I have developed advanced laboratories for courses in computer architecture; the one on instruction pipelining (see conference paper 14 in Section 5.3) is a good example. It has been used in classes at Lund University and Chalmers University of Technology for a couple of decades that gives a token for its fundamental nature!

- I have offered several tutorials and graduate courses at summer schools (CNRS, France, 1994; ARTES, Stockholm, Sweden, 1998), institutions (UPC Barcelona, 1998, 2002), companies (Ericsson 1998), and conferences (EuroPar95 and EuroPar97), as well as being an invited speaker on educational issues (the IEEE CAEWS workshop).
- I gave a two-week intensive Ph. D. course (24 hours) on shared-memory multiprocessors at UPC in Barcelona in April 2002.
- I gave a course on chip multiprocessors in Italy (http://escher.elis.ugent.be/hipeac/summerschool/) in conjunction with the 1st HiPEAC summer school, July 2005.
- I gave a course on "Methods to Transfer Research To Business" with Andrzej Brud of Chalmers Innovation at the 5th HiPEAC summer school, July 2010.
- I gave a 15-hour PhD course at Beihang University in Beijing on Advanced Topicsin Computer Architecture between Oct 8-15, 2014.
- I gave a course at the UPMARC PhD summer school on compression in the memory hierarchy in 2017.
- I gave a course on the ACM Summer School, held in Barcelona in July 2019, 2022 and 2023 on cache coherency and compression in the memory hierarchy.
- In 2012 Professor David Black Schaffer of Uppsala University inspired me to try out the flipped classroom methodology in my computer architecture course. I recorded all my lectures on Youtube and reshaped the course using the flipped classroom approach. It was very well received by the students and I could notice that the results in the exam improved. The students especially liked to have access to the recorded lectures when they were preparing for the exam.
- In 2016, I was asked to develop two MOOCs for Chalmers based on my courses: one basic and one advanced. This was one of the most inspiring tasks (and also laborious) I have done. Coached by the fantastic blended-learning team at Chalmers I developed first a basic course which centers on energy-efficient programming. It was launched at the edX platform in the fall of 2016. The second course, on advanced computer architecture, was launched on edX in January 2017. Both courses have been well-received and they have been delivered regularly at the department since then (2023).
- In 2017, I architected a new Master's program on High-Performance Computer Systems. This program was launched in 2019.

6. Publications

Textbooks

1. L. Ohlsson and Per Stenström: "Computer Organization and Assembly Language Programming," Studentlitteratur and Chartwell-Bratt, ISBN 91-44-26461-5, January 1987.

2. Per Stenström: ''68000 Microcomputer Organization and Programming," Prentice-Hall, ISBN 0-13-584855-5, September 1992.

3. Michel Dubois Murali Annavaram, and Per Stenström. *Parallel Computer Organization and Design.* Cambridge Press. 1st Edition. 2013.

4. Somayeh Sardashti, Angelos Arelakis, Per Stenstrom, David Wood. A Primer on Compression in the Memory Hierarchy. Morgan-Claypool, 2015

5. Michel Dubois Murali Annavaram, and Per Stenström. *Parallel Computer Organization and Design.* Cambridge Press. 2nd Edition. 2024

Journal Papers

1. P. Stenström: "Reducing Contention in Shared-Memory Multiprocessors," in *IEEE Computer*, Vol 21, No 11, pp. 26-37, November 1988.

2. P. Stenström: "A Survey of Cache Coherence Schemes for Multiprocessors," in *IEEE Computer*, Vol 23, No 6, pp. 12-24, June 1990.

3. H. Grahn, P. Stenström, and M. Dubois: "Implementation and Evaluation of Update-Based Cache Protocols Under Relaxed Memory Consistency Models," in *Future Generation Computer Systems*, Vol. 11, No. 3, pp. 247-271, June 1995.

4. F. Dahlgren and P. Stenström: "Using Write Caches to Improve Performance of Cache Coherence Protocols in Shared-Memory Multiprocessors," in *Journal of Parallel and Distributed Computing*, Vol 26. No 2, pp. 193-210, April 1995.

5. F. Dahlgren, M. Dubois, and P. Stenström: "Sequential Hardware Prefetching in Shared-Memory Multiprocessors," in *IEEE Trans. on Parallel and Distributed Systems,* Vol. 6 No 7, pp. 733-746, July 1995.

6. M. Dubois, J. Skeppstedt, and P. Stenström: "Essential Misses and Memory Traffic in Coherence Protocols," in *Journal of Parallel and Distributed Computing*, Vol. 29, No 2, pp. 108-125, October 1995.

7. F. Dahlgren and P. Stenström "Evaluation of Stride and Sequential Hardware-based Prefetching in Shared-Memory Multiprocessors*,"* in *IEEE Trans. on Parallel and Distributed Systems,* Vol. 7, No. 4, pp. 385-398, April 1996.

8. M. Brorsson and P. Stenström: "Characterising and Modelling Shared-Memory Accesses in Multiprocessor Programs," in *Parallel Computing*, No 22, pp. 869-893, 1996.

9. P. Stenström, M. Balldin, and J. Skeppstedt: "The Design of a Non-Blocking Load Processor Architecture," in *Microprocessors and Microsystems, No 20, pp. 111-123,* 1996.

10. H. Grahn and P. Stenström: "Evaluation of an Adaptive Update-Based Cache Protocol," in *Journal of Parallel and Distributed Computing*, 39(2):168-180, December 1996.

11. J. Skeppstedt and P. Stenstrom. Using Dataflow Analysis Techniques to Reduce Ownership Overhead in Cache Coherence Protocols. In *ACM Transactions on Computer Systems,* Vol. 18, No 6., pp. 659-682, November 1996

12. P. Stenström, M. Brorsson, F. Dahlgren, H. Grahn, and M. Dubois: "Boosting Performance of Shared-Memory Multiprocessors," in *IEEE Computer,* pp. 63-70, July 1997.

13. M. Karlsson and P. Stenström: "Effectiveness of Dynamic Prefetching in Multiple-Writer Distributed Virtual Shared Memory Systems," in *Journal of Parallel and Distributed Computing*, Vol. 43, No. 2, pp. 79-93, 1997.

14. F. Dahlgren, M. Björkman and P. Stenström: "Reducing the Read Miss Penalty for Flat COMA Protocols, in *the Computer Journal*, Vol. 40, No. 4, pp. 208-219, 1997.

15. P. Stenström, Erik Hagersten, David Lilja, Margaret Martonosi, and Madan Venugopal: “Trends in Shared-Memory Multiprocessing,” in *IEEE Computer*, Vol. 30, No. 12, pp. 44-50, December 1997.

16. F. Dahlgren, J. Skeppstedt, and P. Stenström: “An Evaluation of Hardware-Based and Compiler-Controlled Snooping Cache Protocol Extensions,” in *Journal of Future Generation Computer Systems,* No. 13, pp. 469-487,1998.

17. F. Dahlgren, M. Dubois, and P. Stenström: “Performance Evaluation and Cost Analysis of Cache Protocol Extensions for Shared-Memory Multiprocessors,” in *IEEE Transactions on Computers*, Vol. 47, No 10, pp. 1041-1055, Oct. 1998.

18. J. Skeppstedt, F. Dahlgren, and P. Stenström: “Evaluation of Compiler-Controlled Updating to Reduce Coherence-Miss Penalties in Shared-Memory Multiprocessors,” in *Journal of Parallel and Distributed Computing,* Vol. 56, No 2, pp. 122-153, 1999.

19. T. Lundqvist and P. Stenström: “An Integrated Path and Timing Analysis Method Based on Cycle-Level Symbolic Execution,” In *Journal of Real-Time Systems,* 17 (2/3):183-207, November 1999.

20. H. Grahn and P. Stenström: “Comparative Evaluation of Latency-Tolerating and Reducing Techniques for Hardware-Only and Software-Only Directory Protocols”, *Journal of Parallel and Distributed Computing,* Vol. 60, No. 7, pp. 807-834, July 2000.

21. J. Jalminger and P. Stenström “Improving Energy-Efficiency in Off-Chip Caches using Selective Prefetching”, In *Journal of Microprocessors and Microsystems*, No 26, pp. 107-121, 2002.

22. P. Rundberg and P. Stenström: An All-Software Thread-Level Data Dependence Speculation System for Multiprocessors,” *Journal of Instruction-Level Parallelism*, Vol 3. Oct 2002.

23. Håkan Grahn and Per Stenström. A Comparative Evaluation of Hardware-Only and Software-Only Directory Protocols in Shared-Memory Multiprocessors, *Journal of Systems Architecture*, Vol 50 (2004) pages 537-561.

24. Jonas Jalminger and Per Stenstrom: A Cache Block Reuse Prediction Scheme. *Journal of Microprocessors and Microsystems.* Vol 28 (2004), pages 373-385.

25. K. De Bosschere, G. Gaydadjiev, X. Martorell, N. Navarro, M. O’Boyle, D. Pnevmatikatos, A. Ramirez, P. Sainrat, A. Seznec, P. Stenstrom, and O. Temam. High-Performance Embedded Architecture and Compilation Roadmap. In *Transactions on High-Performance Embedded Architectures and Compilers.* Vol 1, No 3. Dec. 2006.

26. J. Chen, M. Dubois, and P. Stenstrom: Integrating Complete-system and User-level Performance/Power Simulators: the SimWattch Approach. In *IEEE Micro* Magazine, July-August, 2007.

27. J. Hollmann, A. Ardo, Per Stenstrom: The Effectiveness of Caching in a Distributed Digital Library. In *Journal of System Architecture,* pages 53(7) 403-416, 2007.

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7. Postdocs, Ph.Ds and Licentiates

Post-docs advised

Rubén Gonzalez (2010 – 2012)

Rubén Titos (2012 – 2014)

Miquel Pericas (2014 – 2016)

Vassilis Papaefstathiou (2014 – 2016)

Risat Pathan (2014 – 2016)

Madhavan Manivannan (2018 –

Bhavishya Goel (2019 –

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8. Jim Nilsson: "*Towards Accurate and Resource-Efficient Coherence Prediction*" Ph. D. thesis (main advisor), Department of Computer Science and Engineering, Chalmers University of Techology, January 2004. First Employment: Startup company.
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13. Mafijul Md. Islam. "*Techniques to Cancel Execution Early to Improve Processor Efficiency*". Ph. D thesis (main advisor). Department of Computer Science and Engineering, Chalmers University of Technology, June 2011. First employment: Volvo Technology.
14. Anurag Negi. "*Speculative State and Contention Management in Hardware Transactional Memory*". Ph. D. thesis (main advisor). Department of Computer Science and Engineering, Chalmers University of Technology, March 2013. First employment. NVIDIA. Portland, Oregon, U.S.A.
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20. Petros Voudouris "*Scheduling techniques to improve the worst-case execution time of real-time parallel applications on heterogeneous platforms*" (main advisor, co-supervised by Risat Pathan). Department of Computer Science and Engineering, Chalmers University of Technology, May 2021.
21. Muhammad Waqar Azhar. "*Techniques to Improve Energy Efficiency on Heterogeneous Multiprocessors under Timing and Quality Constraints*" (main advisor, co-supervised with Miquel Pericàs, Vassilis Papaefsthatiou and Madhavan Manivannan). Department of Computer Science and Engineering, Chalmers University of Technology. March 2022.
22. Mehrzad Nejat. "Dynamic Management of Multi-Core Processor Resources to Improve Energy Efficiency under Quality-of-Service Constraints" (main advisor; co-supervised with Miquel Pericàs and Madhavan Manivannan). Department of Computer Science and Engineering, Chalmers University of Technology. May 2022.
23. Nadja Ramhoj Holtryd "Adaptive Microarchitectural Optimizations to Improve Performance and Security of Multi-Core Architectures" (main advisor; co-supervised with Miquel Pericàs and Madhavan Manivannan) Department of Computer Science and Engineering, Chalmers University of Technology. February 2023.

Licentiate Theses (A Swedish degree half-way between the MSc. and Ph. D. degree)

1. Magnus Broberg: "*An Approach to Tune Performance of Multithreaded Programs on Multiprocessors*," Licentiate thesis (examiner, main advisor: Lars Lundberg), Department of Computer Science, University of Karlskrona/Ronneby, June 1999.
2. Ulf Assarsson: "*View Frustum Culling and Animated Ray Tracing: Improvements and Methodological Considerations"*, Licentiate thesis (main advisor, co-advised by Dr. Tomas Möller). May 2001.
3. Jonas Jalminger. "*On Improving Data Cache Space Utilization*", Licentiate thesis (main advisor), Jan 2002.
4. Martin Kampe. "*Prediction Methods for Cache and Branch Management in Computers,* Licentiate thesis (main advisor, co-advised by Dr. Fredrik Dahlgren, and Prof. Michel Dubois), May 2002.
5. Peter Rundberg. "*Data Dependence Speculation Methods to Expose Thread-Level Parallelism* (main advisor), Nov 2002.
6. Jochen Hollman "*Latency Reduction and Tolerance in Distributed Digital Libraries*" (main advisor, co-advised by Dr. Anders Ardö) Sept 2003
7. Nima Namaki. *"Dominated Performance: Methodology, Tools and Empirical Experiments.* (main advisor, co-advised by Stefan Christiernin), December 2008.

8. Professional Service

8.0 Others

- Appointed ACM Distinguished Speaker 2023 on a 3-year term

8.1 Editorial Service

- On the Search Committee for a new Editor-in-Chief of IEEE Transactions on Sustainable Computing. 2024
- Launch of an experiment regarding a journal-first publication model in cooperation between ACM TACO and the 2012 edition of the HiPEAC conference. Acting as editor for the special issue together with Koen De Bosschere in 2012-2014.
- Appointed as Senior Associate Editor in ACM TACO because of the accomplishments with the new publication model together with Koen De Bosschere. Since 2014-
- Editor of the HiPEAC Newsletter together with Dr. Rubén Titos Gil and Dr. Miquel Pericàs, 2012-2016
- Associate Editor-in-Chief (Computer Architecture) for Journal of Parallel and Distributed Computing. Since 2011-
- Associate and Topical Editor of IEEE Transactions on Computers, Since 2019
- Associate Editor ACM Transactions on Architecture and Code Optimization (TACO) since 2011.
- Editor-in-chief, Transactions on High-Performance Embedded Architectures and Compilers *Transactions on HiPEAC*, 2004-2010
- Editor of IEEE Transaction on Computers, between March 2000-2004
- Editor of IEEE Transactions on Parallel and Distributed Systems. November 2008- 2011.
- Editor (area: shared-memory multiprocessors) for JPDC (Journal of Parallel and Distributed Computing) 1993-2011.
- Editor of the Journal of Universal Computer Science since 1994; one of the first electronic journals in the field.
- Editor of IEEE/TCCA *Computer Architecture Letters,* 2001-2010.
- Editor of the *International journal of embedded systems,* since February 2004-2009.
- Editor of IEEE Micro, 2016 – 2018. Renewed 2019 – 2020.
- Editor of Springer Nature Journal of Computer Science (2019 –)
- Associate Editor and Topical Editor of IEEE Transactions on Computers (2019 –)
- Guest editor for “Applications for Shared-Memory Multiprocessors” in the December 1996 issue of IEEE Computer together with Dr. Fredrik Dahlgren.
- Guest editor for “Distributed Shared-Memory Multiprocessors” in the Spring issue 1999 of the Proceedings of the IEEE together with Dr. Veljko Milutinovic.
- Guest editor for “Languages, Compilers, and Tools for Embedded Systems” in ACM Transaction on Embedded Computer Systems in March, 2004 together with Dr. Frank Mueller.
- Guest editor for “Transactions on HiPEAC” top papers in 2005 International Conference on High-Performance Embedded Architectures and Compilers, March 2006.

- Guest editor for “Transactions on HiPEAC” top papers in 2007 International Conference on High-Performance Embedded Architectures and Compilers, March 2007.
- Guest editor for a special issue in Journal of Parallel and Distributed Processing “Trends on Heterogeneous and Innovative Hardware and Software Systems” with Sanjay Ranka, Eduard Ayguade, Jesus Carretero and Alba Melo, 2018
- On the Editorial Committee for selecting the articles of the Dec 2004 issue of IEEE Micro Magazine on Top Picks in Computer Architecture.
- On the Editorial Committee for selecting the articles of 2012 issue of IEEE Micro Magazine on Top Picks in Computer Architecture.
- On the Editorial Committee for selecting the articles of 2019 issue of IEEE Micro Magazine on Top Picks in Computer Architecture.
- Guest editor (together with Viktor Prasanna and Yves Robert) on a special issue in JPDC (scheduled for publication in JPDC 74(6), 2014) on What’s Next.
- Guest editor (together with Alba Melo and others) on a special issue in JPDC on the best of SBAC-PADS, to appear in 2018.
- Guest editor with Onur Mutlu on a Special Issue in IEEE Transactions on Computers on In/Near-memory processing scheduled for October 2023.
- On the CACM SIGARCH Research Highlights Committee chaired by Natalie Enright Jerger. 2023.
- On the advisory board of CCF Transactions on High Performance Computing (Springer Nature) since 2019.
- Chair of the IEEE reappointment committee of the EiC of IEEE Micro 2020

8.2 Chairmanship & Committee Appointments

- Best paper award committee HPCA 2024
- On the ACM SIGARCH Alan Berenbaum Distinguished Service Award Committee (2024-2026)
- SIGARCH/SIGMICRO CARES member 2021-2025
- Co-chair of SIGARCH/SIGMICRO CARES 2022
- Session chair of best paper award session and on the committee ISCA 2022
- On the SIGARCH CACM research highlights committee to nominate the articles to be highlighted from the top venues in Computer Architecture: 2019
- On the SIGARCH CACM research highlights committee to nominate the articles to be highlighted from the top venues in Computer Architecture: 2020
- On the SIGARCH CACM research highlights committee to nominate the articles to be highlighted from the top venues in Computer Architecture: 2022
- Elected as Member-at-Large (2014-2018) in ACM Council
- Elected member of ACM Europe Council since 2014 and as officer (Secretary) 2015 - 2017
- Appointed to be on the ACM Turing Award Committee (The “Nobel Prize” Committee of Computing Sciences) 2013-2018.
- Appointed to be on the ACM SIGARCH Maurice Wilkes Award Committee 2014-2016 (Chairman 2015)

- Appointed to be on the ACM SIGARCH Maurice Wilkes Award Committee 2017 (Chairman) due to a conflict-of-interest situation.
- Appointed to be on the IEEE/ACM Eckert-Mauchly Award Committee 2014-2017 representing ACM and chairman for it in 2015.
- Appointed to be on the IEEE/ACM Eckert-Mauchly Award Committee 2019-2021 representing IEEE CS and chairman for it in 2021.
- On TCCA Member-at large 2020 - 2024
- On the Executive Committee of IEEE TCCA 2023 -
- On the Heidelberg Laureates Forum committee 2013, 2014, 2015, 2016, 2017, 2018.
- On the PRACE scientific committee, 2016 - 2018
- On the Steering Committee of ACM International Conference on Supercomputing, 2014 – 2017
- On the Steering Committee of IEEE/ACM PACT, since 2018
- On the steering committee of the HiPEAC Conference since the beginning in 2005. Since 2008 Steering Committee Chair. Together with Koen De Bosschere we reformed the conference and its publication model in 2012. The Paris venue attracted around 400 participants and the attendance has been growing since that point.
- Minitrack coordinator for “Shared Memory Multiprocessors” in the 27th Hawaiian International Conference on System Sciences, 1994.
- Program vice-chair, 14th IEEE Symp. on Distributed Computer Systems, 1994
- Task force leader for “Trends in Shared-Memory Multiprocessing” in the 30th Hawaiian International Conference on System Sciences, 1997.
- Global chair for the Parallel Computer Architecture Topic of Euro-Par’96 and 2000.
- General chair for the 28th IEEE/ACM Annual International Symposium on Computer Architecture held Gothenburg, July 2-4,2001
- Program chair of ACM/SIGPLAN LCTES’2003 (Languages, Tools & Compilers for Embedded Systems).
- Program vice-chair of Architecture Track of 2004 IEEE International Parallel and Distributed Processing Symposium.
- Program chair of 31st IEEE/ACM Annual International Symposium on Computer Architecture held in Munich, 2004.
- Program vice-chair of the Architecture track of the 2004 ACM Conference on High-Performance Computing.
- Program track chair of the High-Performance Embedded Processor Architecture Track of the 2005 ACM Computing Frontier Conference.
- Program co-chair of 2007 High-Performance Embedded Architecture and Compiler Conference.
- Program co-chair of 2007 ACM Computing Frontiers Conference.
- General co-chair of 2008 High-Performance Embedded Architecture and Compiler Conference.
- Program vice-chair of Architecture Track of 2007 IEEE International Parallel and Distributed Processing Symposium.

- Program co-chair of the 14th IEEE International Symposium on High-Performance Computer Architecture 2008.
- Program chair of the 2009 IEEE International Parallel and Distributed Processing Symposium.
- Program vice-chair of the Computer Architecture and Real-Time Systems Track for the 2010 ACS/IEEE International Conference on Computer Systems and Applications, Tunisia, May 2010.
- Program chair of ACM International Conference on Supercomputing (ICS), 2014.
- Program track chair, architecture, SBAC-PAD 2017
- Program co-chair of IEEE/ACM PACT 2018
- Industry Liaison Co-chair for ISCA 2018
- Organized HiPEAC spring CSW in 2018
- Program area chair – computer architecture – IPDPS 2019 – Rio de Janeiro
- Program co-chair of APPT 2019 in Tianjin, China
- Co-founder of the Swedish Multicore Initiative and its Multicore Day organization from 2007 and onwards. Organizer of the 2010 Multicore Computing Workshop at Chalmers University of Technology.
- Organized Multicore Day in Stockholm 2018.
- Organizer and co-founder of the MULTIPROG Workshop in response to the programmability challenges of the multicore trend held in conjunction with the HiPEAC conference series (2007-2015): First edition on January 27, 2008 in Göteborg, in Paphos Cyprus in 2009 for the second time, in Pisa, Italy in 2010 for the third time, in Heraklion, Greece in 2011 for the fourth time, in Paris in 2012 for the fifth time, then in Berlin 2013, Vienna 2014 and Amsterdam 2015.
- Organizer of the Barcelona Multicore Workshop held in Barcelona June 5-6, 2008
- Member of the Advisory Board of the EUROPAR conference series, since 1995.
- Member of the IEEE TCCA Chair Nomination Committee 2001.
- Member of the advisory committee of IEEE CS TCCA (2001-2005)
- Member of Steering Committee of IEEE/ACM 28th, 29th, 31st, 32nd, and 33rd ISCA
- Member of Steering Committee of IEEE HPCA 2009
- Member of Steering Committee of IEEE IPDPS 2009 and 2010
- Member of Steering Committee of ACM/SIGPLAN LCTES (Languages, Tools & Compilers for Embedded Systems) 2002 - 2006.
- Member of Steering Committee of the Int. Conf. on High-Performance and Embedded Architectures and Compilation (HiPEAC) (since 2005).
- Member of the ACM SIGARCH Distinguished Service Award Committee 2008-2010 and chairman for it in 2010.
- Member of the ACM/IEEE Eckert-Mauchly Award Committee 2004-2007.
- Chairman of Steering Committee for the International Conference on High-Performance and Embedded Architectures and Compilers series. 2007-
- Member of the HiPEAC SC from its start 2004
- Member of Executive Committtee of IEEE TCCA 2011-2016.

- Member of the Executive Committee of IEEE TCCA, 2017-2018
- Member of TCCA Award Committee for the John Cocke Young Investigator Award 2011-2012 (Chairman in 2011).
- On the Board of Governors of ACM SIGARCH 2011-2013
- On the IEEE Computer Society Publications Board (at large) 2012
- On the Council of ACM Europe. Since 2012
- Organized the 2012 HiPEAC Computing Systems Week April 2012.
- On the 2012, 2013, 2014, 2015, 2017, 2018, 2021 IEEE Fellow Committee.
- Member of the Eckert-Mauchly Award Committee (representing IEEE CS) 2014-2017
- Member of the EC of IEEE TCCA since 2015
- Member of TCCA Award Committee for the Young Investigator Award 2019-2021 (Chairman in 2020).
- Chairman of search committee for EiC for ACM TACO, 2019
- Best paper award committee for IEEE HPCA, 2020
- On CARES committee from 2021
- On the IEEE CS Awards Committee 2021
- On the ACM Alan D. Berenbaum Distinguished Service Awards Committee 2024-2026.

8.3 Program Committee Membership - I have served on more than 70 PCs

ACM/IEEE International Symposium on Computer Architecture (ISCA): 1996, 1997, 2000, 2003, 2004 (chair), 2006, 2010, 2011, 2012, 2021, 2022. ERC 2015, ERC 2016, ERC 2017, ERC 2019, ERC 2020. ERC 2024. SIGARCH and TCCA.

IEEE International Symposium on High-Performance Computer Architecture (HPCA); 1996, 1997, 2000, 2001, 2002, 2006, 2008 (program co-chair), 2011, 2012, 2013, 2014 (Proxy PC chair), 2016 (proxy PC chair), 2019, 2017 (ERC) 2018 (ERC), 2020, 2021, 2022 (ERC), 2023.

IEEE Top-pick issue in IEEE Micro Magazine, 2012.

IEEE Top-pick issue in IEEE Micro Magazine, 2018 (2019).

Member of the program committee of the Branch Prediction Competition ISCA 2016

ACM/IEEE Micro: 2004 and 2005. SIGARCH and TCCA. On the ERC 2012, 2015, 2016, 2021, 2022. ERC 2024.

IEEE IPDPS: 2003, 2004 (vice-chair), 2006, 2007 (vice-chair), 2009 (program chair), 2019 (vice chair), 2020 (vice track chair), 2022

IEEE ISPASS 2005 and 2006

IEEE ICDCS 1992 and 1993 (vice-chair)

IEEE PACT 2004, 2007, 2009, 2013, 2014, 2017, 2018 (co PC-chair), 2020

IEEE SPDP 1996

ACM ASPLOS 1996, 2000, 2006, 2012. On review board 2010, 2023 (ERC)

ACM SC 1997

ACM ICS 1998, 2003, 2004, 2005, 2014 (program chair), 2017, 2020

ACM HiPC 2003, 2004 (vice-chair), 2005.

ACM LCTES 2003 (program chair), 2006.

ACM Computing Frontiers 2005, 2007 (program co-chair)

EuroPar 2 1995, 1997 (chair for topic), 1999 (vice-chair for topic), 2000 (chair for topic)

PDCS 1997, 1998, 1999

HIPEAC 2005, 2007 (program co-chair), 2009.

DATE 2006, 2007

SSS 2009

SBAC-PAD 2011, 2016, 2017 (track chair)

ICPP 2022

Roles of Logic in AI Systems? Stanford 2017

MPP 2018

Workshops: CANPC'97 and CANPC'98, EWOMP'99, IEEE Memory Wall workshop (in conjunction with ISCA 2000), MEDEA workshop in conjunction with PACT 2000, 2006, 2007, and 2009. EASY workshop in conjunction with ISCA-2001. MTEAC-6 in conj. with MICRO-35, 2002. dasCMP 2005, dasCMP 2006, dasCMP 2007, dasCMP 2008. MULTIPROG 2008, 2009 and 2010 (in conj. with HiPEAC) as organizer, WRC 2008 and 2009 (in conj. with HiPEAC), WIOSCA'2010 (in conj. with ACM/IEEE ISCA), BMW 2008, 2010.

External review committee (many not documented): Micro 2015

8.4 Reviewing for Scientific Conferences, Journals & Textbooks

Referee for IEEE Computer, IEEE Micro, IEEE Concurrency, Journal of Parallel and Distributed Computing, IEEE Transactions on Computers, IEEE Transactions on Parallel and Distributed Systems, Proceedings of the IEEE, ACM Transactions on Computer Systems, Parallel Computing, IEE Proceedings, Journal of Microprocessors and Microsystems, Journal of Universal Computer Science, Journal of Real-Time Systems, ACM Transactions on Embedded Computer Systems, IEEE/ACM International Symposium on Computer Architecture (ISCA), International Conference on Parallel Processing (ICPP), ACM Supercomputing, IEEE International Conference on Distributed Computing Systems, IEEE International Parallel Processing Symposium (IPPS), IEEE International Symposium on Parallel and Distributed Systems, IEEE International Symposium on High-Performance Computer Architecture (HPCA), ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Euro-Par, Hawaii International Conference on System Sciences, Parallel Architectures and Compilation Techniques (PACT), ACM International Conference on Supercomputing (ICS) ACM Principles of Programming Languages (POPL), International Conference on High-Performance Embedded Architectures and Compilers, Transactions on High-Performance Embedded Architectures and Compilers, and many others.

Review of textbook proposals for Addison-Wesley, Morgan Kaufmann (1997 and 2001), Cambridge University Press, and tutorials for IEEE Computer Society Press.

8.5 Reviewing of Grant Proposals & Applicants for Academic Positions

Review of research grant proposals for the National Science Foundation (NSF) (1991,1997), the Swedish Research Council for Engineering Science (TFR) (1995), the Swedish

Foundation for Strategic Research (1998-1999), and the Norwegian Science Foundation (NFR) (1996-2000),

Chair of evaluation panel in CS for Swedish Research Council 2001-2004.

On the evaluation panel of the priority program on Organic Computing for the German Science Council (DFG), February 2005.

On the panel to evaluate prolongation of research programs in CS for SSF, December-January 2005/2006.

Member of the Swedish Research Council for Research Infrastructure 2012-2015

On the panel of Swedish Foundation of Research in the program of Future Research Leaders, 2019

Elector of Vetenskapsrådet 2015, 2018, 2021 (nomination committee).

Expert evaluations of applications for associate professorships in computer science and engineering at Kristianstad University College (1993), Lund University (1994), Karlskrona/Ronneby University (1995,1999), Chalmers University of Technology (1994, 1997), Royal Institute of Technology (1997, 1998, 2000), Luleå University (1998, 2000), Kuwait University (1998), Uppsala University (1999, 2002), Trollhättan (2003). Mälardalen (docent) 2005, 2008, University of Cyprus (2006, 2012), Linné universitetet Växjö (2012, 2013 – research portfolios for internal funding), Högskolan Väst (2013 - docent), Uppsala University (2014 – docent).

Evaluations for promotion to assistant/associate professor (U.S.A.): Rice university (1998), Cornell University (1998), Princeton University (1999), Rochester Univ. (2001), Rutgers University (2002, 2003), University of Maryland (2003). University of Illinois - Urbana Champaign. (2004), University of Massachusetts, Amherst (2005), Harvard (2009), Penn State (2010), University of Cyprus (2007, 2012) Carnegie Mellon University (2012), North Carolina State University (2012), University of Michigan (2012).

Evaluations for promotion to Reader at Imperial College (U.K.) (2001), Full professor promotion University of Edinburgh (2005), Reader, Edinburgh (2009), Full professor promotion Unversity of Edinburgh (2012), Technion (2016).

Evaluations for promotion to full professor (U.S.A & Canada): University of Minnesota (1999), Georgia Institute of Technology (1999), Rice University (1999), University of Texas at Austin (2000), University of Southern California (2003), University of California, San Diego (2003), Northeastern University (2004), Rochester (2006), CMU (2006), University of Colorado (2008), North Carolina State University (2011), University of Toronto (2012), Princeton University (2012), UC Riverside (2012), UC Santa Barbara (2013), Duke (2014), Rochester (2016), Stanford (2017), Georgia Tech (2017)

Expert evaluations of applicants for full professorships at Luleå Technical University (1996, 2004), the University of Mälardalen (1997,1998,2001), Karlskrona/Ronneby University (1998), Uppsala (1999), Royal Institute of Technology (2000,2003), and Jönköping University (2002), Denmark Technical University (2005) TU Vienna (2015), Uppsala (2017), Royal Institute of Technology (2019), Linkoping (2020), KTH (2021)

Member of a group to establish criteria for applications for promotions to full professors at Uppsala University and Umeå University (1999).

Member of the National Committee for promotion to full professor in Computer Science (1999)

Reviewer and member of evaluation committees of Ph. D. theses at Royal Institute of Technology (1992, 1997, 1998, 2004, 2015, 2020), Uppsala University (1994,1997,2000, 2002, 2006 x3, 2016, 2019, 2020), Chalmers University of Technology (1994,1998,2001,2006), Oslo University (1998), Joensuu University, Finland (1998), University of Paris Sud (2002,2005),

Luleå University of Technology (2000, 2004). IT-university, Göteborg (2004, 2006), Blekinge Institute of Technology (2005, 2014), TU Delft (2006,2011), University of Edinburgh (2008), Murcia (2009), UPC (2010), Vaxjo (2010), DTU (2011), Murcia (2012), EPFL (2013), University of Illinois, UC (2013), FORTH and University of Crete (2013), Ghent University (2014) University of Amsterdam (2015), Tromsö (2019), Lund (2019), Lund (2023), Trondheim – opponent – (2024).

Jury member at Dr. Pascal Sainrat's habilitation dissertation at University of Paul Sabbatier and Institute de Recherche en Informatique de Toulouse, March 1998.

Jury member and referee of Stephane Louise's Ph. D. thesis at University of Paris Sud. Jan 2002.

Jury Member of the Ph.D. dissertation of Christian Fench (Edinburgh, 2008).

Jury Member of Ph. D. dissertation (Manchester 2009).

Faculty opponent at Knut Omang's thesis defense at University of Oslo in June 1998.

Faculty opponent at Uppsala University, May 25, 2000, for Mikael Sjödin.

Faculty opponent at Uppsala University, April 2016.

Faculty opponent at Liv Vran's thesis defense at the Arctic University, Tromsö, Feb 15, 2019.

Member of a committee to define the scope of a new EU-IST program on "Emerging Computing Architectures: New Processor Architectures and Advanced Compiler Technologies" in the spring of 2004.

Recipient of a certificate of belonging to the category of best senior reviewers for IEEE Computer in 1994.

PhD Jury member INRIA/University Paris Sud Daniel Gracia Perez, October 2005.

Reviewer for Vaxjo University for research proposals. Oct 2010, 2013, 2015.

Expert evaluator for EU FP7 IP TeraFlux for the European Commision, 2011, 2012, 2013 and 2014.

Expert evaluator for ERC senior grants (2010, 2011, 2017)

Reviewer of research proposals from Qatar National Research Fund (2011).

On the ERC panel for Computer Science "Consolidator grants", 2014.

On the ERC panel for Computer Science "Consolidator grants", 2016.

On the ERC panel for Computer Science "Consolidator grants", 2018.

On the ERC panel for Computer Science "Consolidator grants", 2020.

On the KK-stiftelse evaluation panel in 2014.

On the KK-stiftelse evaluation panel in 2015. Also as project evaluator 2015

On the KK-stiftelse evaluation panel in 2016. Also as mid-term evaluator 2016

On the KK-stiftelse evaluation panel in 2017. Also as mid-term evaluator 2017

On the KK-stiftelse evaluation panel in 2018. Also as mid-term evaluator 2018

On the KK-stiftelse evaluation panel in 2019. Also as mid-term evaluator 2019

On the KK-stiftelse evaluation panel in 2020. Also as mid-term evaluator 2020

On the KK-stiftelse evaluation panel in 2021.

Reviewer for ERC Synergistic grant proposals: 2019

Reviewer for KAW proposals 2019.

Referee for Research Fellows for the British Royal Society 2015 University Research Fellowship

Habilitation jury member Stephane Louise, Paris 2015

Patent litigation case for Wilmer Cutler Pickering Hale and Dorr LLP in 2015

Evaluation of researchers in Linne University 2015

Evaluation of research proposals for ERC and for Norska forskningsrådet 2017

Evaluation of research proposals for Norska forskningsrådet 2019 (four)

On the ERC panel for Computer Science in 2020

8.6 Other Professional Activities

Moderator on a panel of the 3rd IEEE workshop on Scalable Shared-Memory Multiprocessors in San Diego, May 1993.

Moderator on a panel on the 5th IEEE workshop on Scalable Shared-Memory Multiprocessors in Santa Margherita Ligure, Italy, 1995.

Organized a task force on "Architectural Trends for Shared-Memory Multiprocessors" in conjunction with HICSS'97 Wailea, Hawaii.

Panelist at the IEEE workshop CANPC'98 in conjunction with HPCA'98

Panelist at the IEEE workshop CAECW'2000 in conjunction with HPCA'2000

Organized a panel at the Sixth Swedish Workshop on Computer Systems Architecture, Gothenburg, May 1998.

Organized a panel at IPDPS 2007 on Multi-core issues.

Organized a panel at IPDPS 2011 on the Future of Computing

8.7 University Services

Was an expert in the procurement committee of a supercomputer platform at Chalmers to service computational scientific problems in virtually all disciplines at Chalmers (1996-1997)

Participated in the development of D++, a new education program in Computer Science and Engineering. Specifically, I designed a specialization in Computer Systems (1995-1999).

I acted as a chair of the council for the faculty of the School of Electrical Engineering and Computer Science (1998-1999).

I was part of a working group to review Forskning 2000, a governmental evaluation of the research policy for the next decade (1999).

I was vice-dean of the School of Electrical and Computer Engineering with responsibility of the Ph. D. Education between 1999-2002.

I was vice-dean of the School of Computer Science and Engineering with responsibility of the Ph. D. Education between 2002-2003.

I was member of the faculty council between 1999 and 2002.

I was part of a working group to provide the government with input for strategic research actions, Dec 1999.

I was a member of the recruitment committee at the School of EEC and M&CS from May 2000 and Jan 2001, resp. until 2002. Between 2002 until 2005, I held the same position in the school of CSE.

I was the chair of the faculty search committee at the IT University of Goteborg between 2002-2005 and continued to serve this committee until 2007.

I was the chair of the research committee at the School of Electrical and Computer Engineering, from June 2000 until 2002.

I was on the steering committee for the planning of the IT-University in Goteborg between 2000 and until a permanent organization was formed in 2002.

I was on the admission committee for selecting 3rd-grade students at the engineering programs for studies at foreign partnership universities (2001-2003)

I was on the steering committee for student recruitment strategies at Chalmers, 2001-2002.

I was leading the departmental recruitment group to be responsible for the process of recruiting (non-tenured) assistant professors to the department and to provide recommendations on promotion cases to the department head. 2010-2012.

On a committee at the IT-University to look at the interaction between IT and the different area of advances in 2011.

On a committee to evaluate the applicants for Knut and Wallenberg Fellow to be submitted by Chalmers in early 2012.

On the search committee to recruit a new chairman of the computer science and engineering department in the spring of 2012.

On the faculty search committee for the IT faculty of Gothenburg University. 2012-

Co-chair (with Prof. Aarne Ranta) of the faculty council (to consolidate the view of faculty members) at the Department of CSE, 2013-2015.

On the search committee to recruit a new chairman of the computer science and engineering department in the spring of 2014.

Division head of Computer Engineering, April 2015 –

On the reference group of Research evaluation, (Affe Almroth) 2017

9. International Talks and Lectures - More than a hundred talks abroad

I have delivered more than a hundred international research presentations over the years.

1. Carnegie-Mellon University, Pittsburgh, U.S, Oct. 1986.
2. IBM Yorktown Heights, New York, U.S., Oct. 1986.
3. PARLE conference, Eindhoven, Holland, June 1987.
4. HICCS'21 A Cactus Stack Multiprocessor Memory Organization" HICSS'21 conference, Hawaii, U.S., Jan. 1988.
5. N.E.C. Corporation, Kawasaki, Japan, Dec. 1988.
6. International seminar on performance of distributed and parallel systems, Kyoto, Japan, Dec. 1988.
7. 16th ISCA, Jerusalem, Israel, June 1989.
8. Hebrew University, Jerusalem, Israel, Jan. 1990.
9. University of Washington, Seattle, U.S., Sept. 1990.

10. Ready Systems Inc., Sunnyvale, U.S., Sept. 1990.
11. U. C. Berkeley, Berkeley, U.S., Sept. 1990.
12. Stanford University, Stanford, U.S., Sept. 1990.
13. International Computer Science Institute (ICSI), Berkeley, U.S., Sept. 1990.
14. University of Southern California, Los Angeles, U.S., Sept. 1990.
15. Dolphin Server Technology A/S, Oslo, Norway, Nov. 1990.
16. Oslo University, Oslo, Norway, Nov. 1990.
17. University of Edinburgh, Edinburgh, U.K., May 1991.
18. Stanford University, Stanford, U.S., June 1991.
19. Intel Corporation, Santa Clara, U.S., Dec. 1991.
20. 20th International Conference on Parallel Processing, Chicago, 1991.
21. University of Southern California, Los Angeles, U.S., Dec. 1991.
22. International Parallel Processing Symposium, Los Angeles, U.S., March 1992.
23. 19th ISCA, Gold Coast, Australia, May 1992.
24. Stanford University, Stanford, U.S., Jan. 1993.
25. M.I.T., Cambridge, U.S., Jan. 1993.
26. New York University, New York, U.S., Jan. 1993.
27. ICSEE'93 conference, San Diego, Jan. 1993.
28. University of Southern California, Los Angeles, U.S., Jan. 1993.
29. 3rd Workshop on Scalable Shared-Memory Multiprocessors, San Diego, U.S., May 1993. Moderator on a panel.
30. University of Michigan, Ann Arbor, U.S., April 1994.
31. 4th Workshop on Scalable Shared-Memory Multiprocessors, Chicago, U.S., May 1994.
32. G.M.D., Berlin, Germany, June 1994.
33. Ecole d'ete des jeunes chercheurs (summer school), Toulouse, France, July 1994. (Invited)
34. University of Southern California, Los Angeles, U.S., January 1995.
35. Stanford University, Stanford, U.S., January 1995.
36. Tech talk at Sun Microsystems, Menlo Park, U.S., January 1995. (Invited)

37. 5th Workshop on Scalable Shared-Memory Multiprocessors, Santa Margherita Ligure, Italy, June 1995.

38. University of Washington, Seattle, U.S, Sept. 1995 (Colloquim, invited)

39. University of Southern California, L.A., U.S, Sept 1995

40. Digital Equipment Corporation WRL, Palo Alto, U.S. Sept 1995.

41. University of Pisa, Feb. 1996.

42. Hawaii International Conference on System Sciences, Wailea, Maui, Jan. 1997

43. Gave a tutorial at EUROPAR'97, Aug. 1997, in Passau, Germany (Invited)

44. Invited talk at EUROPAR'97, Aug. 1997 in Passau, Germany

45. Invited talk at INFOFEST'97 in Montenegro, Jugoslavia, Sept. 1997.

46. Panelist at CANPC'98 in conjunction with HPCA'98, Las Vegas, Feb. 1998 (Invited).

47. Gave a tutorial at Technical University of Catalunya, Barcelona, Spain, Feb 1998. (invited)

48. Universitet Paul Sabatier (and IRIT), Toulouse, France, March 1998.

49. Ericsson Research, Älvsjö, April 1998.

50. 1998 IEEE Workshop on Computer Architecture Education in conjunction with 25th ISCA in Barcelona, June 1998. (Invited)

51. ARTES Summer school, Lidingö Stockholm, Aug. 1998. (invited)

52. Sun Microsystems, Menlo Park, CA, Sept. 1998.

53. Research overview at the Winter Meeting for CS Dept., Chalmers, Smögen, Jan 1999

54. Thread-Level Data Speculation Techniques, Ericsson Research, Älvsjö, April 12, 1999

55. All-Software Thread-Level Data Speculation Systems, Dagstuhl Seminars, April 21, 1999 (Invited)

56. Polytechnic University of Barcelona, "On the Interaction between Commerical Workloads and Memory Systems in High-Performance Servers," Sept 9, 1999.

57. University of Maryland, "On the Interaction between Commerical Workloads and Memory Systems in High-Performance Servers," Colloquim, Invited talk, Sept 16 1999.

58. University of Southern California, "On the Interaction between Commerical Workloads and Memory Systems in High-Performance Servers," Sept 20, 1999.

59. Princeton University, "On the Interaction between Commerical Workloads and Memory Systems in High-Performance Servers," Sept 22, 1999.

60. Panelist at CAECW at HPCA-6 in Toulouse, January 9, 2000.

61. ETH, Switzerland, Colloquium, June 8, 2000 “Access Latency Reduction and Hiding Techniques for High-Performance Computers”. (Invited)

62. ETH, Switzerland, June 9, 2000 “Boosting Energy-Efficiency for Off-Chip Caches using Small Block Sizes and Selective Prefetching”.

63. Imsys AB, Stockholm, Aug 7, 2000 “Challenges in Computer Architecture”

64. “Understanding Performance Bottlenecks in Complex Computer Systems” (invited talk), First Summer school on Engineering of Complex Computer Systems, Skövde University, Aug. 15., 2000.

65. Metoder för effektivt utnyttjande av multiprocessorteknologi i transaktionsorienterade system: Project presentation at the NUTEK program conference, Lund, Sept. 11, 2000.

66. Opening address at IEEE/ACM Int Symp. on Computer Architecture (ISCA-2001) July 2, 2001 in Gothenburg.

67. “Can We ever Dream of Making Multiple Processors and Caches Appear as a Simple and Single Entity to the Software” Keynote speech at ICPP-01 on Sept 7, 2001. Valencia, Spain. (Invited)

68. “All-Software Thread-Level Data Speculation on Multiprocessors” Invited talk at University of Paris-Sud XI, Jan 21, 2002.

69. Lecture series in Parallel Computer Architecture. Technical University of Catalonia, Barcelona. April 2002. (Invited)

70. Keynote Talk at IPDPS-2003 (Invited)

71. Distinguished Lecture Talk at University of Southern California, January, 2003 (Invited)

72. Several talks at Sun Microsystems during spring 2003 during my sabbatical there.

73. Colloquium at University of Texas, Austin, April 7, 2003. (Invited)

74. NSF Panel, June 2003 (Invited).

75. IT-University, Göteborg, Sept and Oct 2003

76. Lund University, Nov. 2003

77. Keynote speech at ACM HiPC’2003 in Hyderabad (India), December 20, 2003 (Invited)

78. Sun Microsystems, Feb 9, 2004

79. Computing Frontier conference, Ischia, Italy, April 15, 2004 (Invited)

80. Opening Address at 31st International Symp. on Computer Architecture, Munich, June 2004.

81. Sun Microsystems, August 9, 2004

82. “A Robust Memory Compression Scheme” (Invited) University of Illinois Urbana-Champaign, December 2004.

83. ACACES 2005. Summer school arranged by HiPEAC on Chip-multiprocessors. July 2005, Italy. (Invited)

84. Sun Microsystems, Nov 2, 2005.

85. Keynote speech at the First HiPEAC conference, Barcelona, Nov. 18, 2005. (Invited)

86. Keynote speech at 12th IEEE Symposium on High-Performance Computer Architecture, Feb 14, 2006, Austin Texas.

87. Sun Microsystems, Feb 16, 2006.

88. Multi-core Expo, Munich, Nov 16-17, 2006, invited talk

89. EU FP7 conference, invited talk at session on Computing Systems, Nov 21-22, 2006, Helsinki

90. Moderated a panel on Multi-core challenges at IPDPS 2007.

91. Invited talk at DATE on future of computer architecture, April 17, 2007.

92. Invited talk at Google, Trondheim, Norway, May 3, 2007

93. Invited talk at Ericsson AB, May 24, 2007

94. Invited talk at BSC/UPC Barcelona, July 31, 2007

95. Invited talk at Stamatis Vassiliadis Symposium, Delft, Sept 28, 2007

96. Talk at FET ICT Consultation workshop on "Massive ICT Systems", Brussels, November 7, 2007.

97. Talk at EU IST FP7 Consultation workshop on "High-Performance Computing Systems", Brussels, Dec 17, 2007.

98. Invited talk at University of Edinburgh, May 12, 2008.

99. Invited talk at the Barcelona Multicore Workshop, June 5, 2008

100. Panelist on a panel arranged by Yale Patt at the Barcelona Multicore Workshop, June 5, 2008

101. HiPEAC presentation at EU meeting in Seoul Korea, June 16, 2008 (invited)

102. Keynote presentation at ISCA workshop, June 21, 2008, Beijing, China.(invited)

103. Presentation at Multicore Days Stockholm September 11-12, 2008

104. Panelist at Multicore Days, Stockholm Sept. 11-12, 2008

105. Talk in Lund on October 17.2008

106. Presentation at "Multicores: Theory and Practice" in the EU project ACTORS at Technical University of Kaiserslautern, Germany October 28, 2008

107. Panelist at the SMART 2009 workshop held in conj. with 4th Int. Conf on HiPEAC, Cyprus 2009.

108. Panelist at the 2009 International Parallel & Distributed Processing Symposium.

109. Gave a talk at Multicore Day in Kista on September 15, 2009 on how to use Nema Labs technolgy to make the code multicore ready.

110. Gave a talk at PACT 2009 on our work on Zero-Value Caches. Sept. 2009

111. Gave a talk at SC 2009 on the FASThread technology. Nov 2009

112. Gave a talk at University of Washington on the FASThread technology. Nov 2009

113. Gave a course on business idea identification at ACACES HIPEAC Summer school, July, 2010

114. Participated on a panel at SAMOS 2010, July 19-22, 2010.

115. Gave a talk at the ICT2010 European IST event in Brussels Sept 28, 2010.

116. Panel at BMW Barcelona, Oct 21., 2010. Moderator: Avi Mendelson, Microsoft.

117. Panelist at Workshop on Computer Architecture Education in conjunction with 2011 HPCA.

118. Föreläsning på Rotary i Göteborg "Mikroprocessorn: Maximal Drivkraft i Minimalt Format" 7 februari, 2011.

119. Invited talk at University of Texas at Austin "Scalability Challenges for Future Chip Multiprocessor Architectures" February 17, 2011

120. Keynote at 2011 International Conference on Architectures of Computing Systems. Feb 24, 2011

121. Invited talk at the 2011 Spring Industrial HiPEAC Workshop on Research in Academia and Industry: Insights from Nema Labs. April 6, 2011.

122. Popular lecture at Vetenskapsfestivalen 2011.

123. Moderator for "Looking Ahead" Panel at 25th IPDPS. May 2011 Anchorage.

124. Invited talk at Multicore Day in Stockholm (Sept 15, 2011): Scheme: Software Abstractions for Heterogeneous Multicore Systems.

125. Organizer of the EuReCCA workshop in Barcelona on November 4, 2011

126. Organizer of the HiPEAC Spring Computing Systems Week in Göteborg, April 2012

127. Invited talk at MATEO 2012. June 29, 2012.

128. Invited talk at USC, November 2012.

129. Invited talk at Workshop on Transfer to Industry and Startup (TISU) in conjunction with 9th HiPEAC. January 2013.

130. Invited talk, University of Delaware, May 10, 2013
131. Keynote at Gompute in Göteborg, 2013 (invited), April
132. Keynote at PACT, Edinburgh (invited), 2013, September.
133. Keynote APPT Conference (invited), 2013, August.
134. Invited talk Multicore Day September 2013.
135. Talk at Google on Cache Compression. (20 December 2013).
136. Invited talk for DATE 2014 Hot Topic Session on Dark Silicon, March 27, 2014
137. Invited talk at UIUC May 12, 2014 (host: Josep Torrellas)
138. Invited talk at Ghent University May 27, 2014 (host: Lieven Eeckhout)
139. Invited talk at FORTH, Crete July 10, 2014 (host: Manolis Katevenis)
140. Invited talk at University of Texas at Austin (Yale-75), September 19, 2014
141. Invited talk at ICT, Academy of Science, Beijing, China, Oct 9, 2014
142. Invited talk at IBM Research, Beijing, China, Oct 10, 2014
143. Invited talk at Beihang University, Beijing, China, Oct 12, 2014
144. Invited talk at Xi'an Jiaotong University, Xi'an, China, Oct 15, 2014
145. Blaze memory. Presentation at the Euroserver workshop in conj. w. HiPEAC, Jan 20, 2015
146. Talk at Stanford University March 23, 2015
147. Talk at Google, March 23 2015
148. Talk at Qualcomm in San Diego, March 24, 2015
149. Talk at AMD in Santa Clara, March 25, 2015
150. Talk at NVIDIA, March 26, 2015
151. Talk at Oracle, March 26, 2015
152. Vetenskapsfinalen 2015 "Snabba och gröna datorer", April 19, 2015
153. Keynote at HiPEAC CSW in Oslo, May 6, 2015
154. Zeropoint Memory Systems, technical talk at Facebook, Menlo Park, CA, June 23, 2015
155. Zeropoint Memory Systems, technical talk at Samsung, Mountain View, CA, June 24, 2015
156. Invited talk at the MULTIPROG workshop in conjunction with HiPEAC 2016, Jan 18 2016

157. Invited talk at the “MICROSERVER: Energy-efficient microservers” workshop in conjunction with HiPEAC 2016, Jan 20, 2016

158. Invited talk at ROMOL 2016 in conjunction with HPCA 2016

159. Talk at HPC Summit May 10, 2016

160. Invited talk at the NSF workshop WASEA on future research trends for compilers and architecture in conjunction with PACT, September 2016.

161. Talk at HPC Summit in Barcelona, May 2017.

162. Talk at Huawei, June 2017

163. Summer school class at UPMARC June 2017

164. Samos July 2017

165. Panel speaker at the ACM Conference, September, 2017

166. Talk at ACM Conference on EuroLab-4-HPC, 2017

167. Talk at Rio University, October, Brazil, 2017

168. Panel speaker at SBAC-PAD 2017 in Campinas, Brazil. Oct. 2017

169. Keynote speaker at MCC, Uppsala, December 2017

170. Energiseminarium. SO Energi. IKT är en energislukare. 14 december, 2017

171. Keynote talk at the 17th International Symposium on Parallel and Distributed Computing, Geneva from 25th to 27th of June, 2018.

172. ROMOL Invited talk Barcelona, March 2, 2018

173. HPC Summit 2018

174. Invited talk at Multicore Day, Nov 26 2018.

175. Invited talk at Technion, November 2018

176. Invited talk at Intel, Haifa, November 2018

177. Invited talk at DATE 2019

178. Invited talk at HiPEAC CSW spring edition in Edinburg 2019 (Parallelism management)

179. Invited talk at HiPEAC CSW spring edition in Edinburg 2019 (Innovation)

180. Invited talk at SIAT institute, Chinese Academy of Science, May 2019

181. Invited talk RISC V Conference, June 2019.

182. Invited talk at Yale anniversary in Barcelona July 2, 2019

183. ACM summer school, July 2019, lecturer

184. UC Berkeley September 2019

185. Talk at WASP4ALL, November 2019.

186. Virtual talk (via zoom) at University of Heidelberg, June 2020

187. On the MICRO 2021 panel on "Microarchitecture research: The view from the Globe". Sept 2021.

188. Invited talk at DATE 2022 on technology transfer. March 2022

189. On the panel of 4th Undergrad Architecture Mentoring Workshop (uArch) at ISCA 2022

190. ACM summer school, September 2022, lecturer

191. Keynote address, December 2022, ACM HiPC, Bangalore

192. Invited talk at IIS in Bangalore, December 22.

193. Invited talk in the Distinguished Speaker program at Shanghai Jiao Tong University, December 2022

194. Invited talk at the DAC Supercomputing Center in Bangalore, December 2022

195. ACM summer school, July 2023

196. Keynote speech at the 2023 China Computer Federation Systems Conference, August 5, 2023.

9. Awarded Research Grants

Research projects (grants)

The first name corresponds to the P.I.

Lars Philipson and Per Stenström: *Laboratory of Experimental Computer Architecture*, 1990-1993, STU, about 2.4 MSEK

Lars Philipson and Per Stenström*: Laboratory of Experimental Computer Architecture*, 1993-1996, NUTEK, about 1.8 MSEK.

Per Stenström: *Scheduling of Memory Instructions for Shared-Memory Programs*, 1994-1997, TFR, about 1 MSEK

Per Stenström and Per Andersson: *ATM-based Multiprocessor Interconnects*, 1994-1996, NUTEK, about 800 KSEK.

Per Stenström: *Performance Prediction Testbed for Mobile Packet Data Applications*, 1996-1997, NUTEK. about 700 KSEK

Per Stenström: *Methodologies and techniques to estimate worst-case execution time*. 1997-2002. TFR, about 1.8 MSEK.

Per Stenström, Bengt Nordström, and Mats Viberg: Equipment grant from FRN, about 3,5 MSEK, 1997-2000.

Per Stenström: *A New Approach to Memory Hierarchy Management in Shared-Memory Multiprocessors*. TFR/SSF, about 1.5 MSEK, 1998-2001

Per Stenström: Donation of an E4000 multiprocessor server from Sun Microsystems. About 1 MSEK

Per Stenström. Collaborative Research on Multiprocessors for Database systems. CR with Sun Microsystems. $50,000 from Sun Microsystems. 1998-2000.

Per Stenström, *Design Strategies for High-Performance Real-time Multimedia Applications on Shared-Memory Multiprocessors*, SSF, about 3 MSEK 1999-2003.

Per Stenström: *A New Approach to Thread-level Data Speculation Execution Models.* TFR, about 1 MSEK, 1999-2001.

Per Stenström, "*Metoder för effektivt utnyttjande av multiprocessorteknologi i transaktionsorienterade system*, NUTEK about 700 KSEK, 2000.

Per Stenström and Anders Ardö "*Networked implementation of a distributed electronic journal collection and full text archive*, NORDUNET-II, about 1 MSEK 2000-2001.

Per Stenström (PI): "*Techniques for Module-Level Speculative Parallelization on Shared-Memory Multiprocessors*, SSF, 720 KSEK, 2000-2001

Per Stenström (primary PI, together with Dr. Fredrik Dahlgren, Ericsson), *Support for Real-Time 3D Graphics for Future Mobile Terminals under Energy/Area Constraints*. SSF, 1.2 MSEK 2000-2004.

Per Stenström and Michel Dubois: *MECCA: Meeting the Challenges in Computer Architecture*, collaboration grant 500 KSEK/year for 2001-2004 from STINT.

Per Stenström. Methods for Adapting the Resource Demands in Computer Architectures under various Demand Objectives. Vetenskapsrådet, 1.8 MSEK, 2003-2006.

Per Stenström (primary P.I.) FlexSoC: A Flexible Platform for System-on-Chip in Embedded Systems. SSF 10 MSEK, 2003-2007.

Per Stenstrom (sole PI): Swedish Research Council 2004-2005. 1 MSEK.

Per Stenström (Mateo Valero coordinator). *HiPEAC: High-Performance Embedded Architectures and Compilation Methods.*. EU Network of Excellence in Computer Architecture. 2004-2008. Leading a major effort as workpackage leader

Per Stenstrom. *Compute Resources to Analyze Future Computer Architectures*. Admission to use the compute resources of SNIC.(2005-2006)

Per Stenström (Stamatis Vassiliadis coordinator). *SARC: Scalable Computer Architecture.* EU Integrated project. 2006-2010. 6 MSEK. Leading a major effort as workpackage leader

Per Stenström (Mateo Valero coordinator). VELOX - A STREP accepted by EU FP7. About 200 000 EU (2008-2010)

Per Stenström (Koen De Bosschere coordinator). HiPEAC-2 Network of Excellence accepted by EU FP7. About 360 000 EU (2008 - 2012). Leading a major effort as workpackage leader

Per Stenström (P.I.) Out-of-Order Thread Speculation. Swedish Research Council (2009 - 2012). 1.5 MSEK.

Per Stenstrom, P.I. (and as co-PIs: Lars Svensson, Sally McKee, Per Larsson-Edefors) CHAMPP. Funded by the Swedish Research Councils with a budget of 3 MSEK (about 300,000 Euro) per year from 2010 - 2014.

Industrial PhD (VR) 2010-2014

Per Stenstrom P.I., Ericsson project 2010, 70 KSEK.

Member of The EURO-TM COST action funded by the European Commission (2011-2014)

Per Stenstrom, P.I. (and as co-PIs: Philippas Tsigas and Ulf Assarsson) SSF grant on software abstractions for heterogeneous multicores. 20 MSEK 2011-2016.

Per Stenstrom, P.I. (together w/ Jan Jonsson as co-PI). Grant for a project with RUAG through NRFP. 1.2MSEK 2012-2014.

Per Stenstrom (P.I.). Funded by the Swedish Research Council 2013-2017. 4.4 MSEK.

Per Stenstrom and Georgi Gaydadjiev (P.I.). FP7 Project Euroserver 2013 - 2016 (about 6 MSEK)

Per Stenstrom (P.I.) European Research Council (ERC) Advanced Grant. 2.3 M Euro (about 20 Million SEK) 2013-2018.

ARTEMIS. EMC^2 (P.I. w/ Ioannis Sourdis)

Per Stenstrom (P.I.) ACE: Approximate Computing Systems. VR, 9 MSEK (2015-2019)

Blaze Memory: Innovations kontoret Väst for interviews with end users, 2015 3 months, 60 KKR.

Per Stenstrom (Coordinator) EuroLab-4-HPC. EC CSA FET 1.4 MEU. (2015-2017)

VINN Verifiering for Blaze Memory, Vinnova, 400 KSEK MSEK for 4 months (2015)

Autonomous systems and software development (David Sands P.I., Per Stenstrom and others co-P.Is.) 2015-2026. 1.8 BSEK.

TETRAMAX 2017 (Granted)

HIPEAC-5 2017 (Granted)

EUROLAB4HPC2 2018 (Granted)

VR Distinguished professor (rådsprofessor) 2019 (Pending)

VR project proposal 2019 (Granted)

WASP project proposal 2019. (Granted conditionally)

HiPEAC-6 2019 (Granted

KAW 2020 (submitted)

SSF 2020 PRIDE granted (28 MSEK over five years)

EuroHPC 2020 “eProcessor” granted (15 MSEK over three years)

EuroHPC PILOT-1 (2021) granted (10 MSEK over three years)

EuroHPC and EPI2 (granted) 2021

WASP (2021) (granted)

WASP twin PhD program (granted) 2021

EPI-2 (granted)

- Swedish Research Council. PRIME. Konstruktionsprinciper för minnesberäknande parallella system. 2019-2023

- Foundation for Strategic Research. PRIDE. Principles for Computing Memory Devices.

- Wallenberg. SCALE-ML: Principles for Scalable Parallel Architectures for Machine Learning. 2020 - 2025

- Wallenberg Foundation. Research expedition Databound Computing. 2022-2027

- Wallenberg Foundation Twin-PhD project. Databound Computing. 2022-2027

- European Processor Initiative (SGA2). 2022-2025

- EU eProcessor. 2021-2025

- EU Pilot-1. 2021 - 2025

- EU HiPEAC 2021 – 2023

- SSF ClassIC

- EU DARE. 2025-2030

Awards and Honors

Awarded the grade of IEEE Fellow in 2007, ACM Fellow in 2008 and AAIA in 2023. In 2009 I became a member of the Royal Swedish Academy of Engineering Sciences and in 2010, I became a member of Academia Europaea. In 2012, I became member of the Royal Spanish Academy of Engineering Science and in 2017 I became a member of the Royal Society of Arts and Sciences in Gothenburg.

Recipient of the 2021 ACM SIGARCH Alan D. Berenbaum Distinguished Service Award for the "creation and successful implementation of the TACO/HiPEAC journal-first review model, and for decades long exemplary service contributions to the field."

Elected Member-at-Large of ACM Council (2014 -2018)

Fellow of the IEEE in 2007. Live Fellow since 2024

Fellow of the ACM in 2008.

Fellow of the Asia-Pacific Artificial Intelligence Association (AAIA) in 2023

Member of the Royal Swedish Academy of Engineering Sciences in March 2009.

Member of Academia Europaea since September 2010.

Member of the Spanish Royal Academy of Engineering since October 2013

Member of the Royal Society of Arts and Sciences in Gothenburg December 2016

Asia-Pacific Artificial Intelligence Association (AAIA)International Artificial Intelligence Industry Alliance (AIIA) 2023

International Artificial Intelligence Industry Alliance (AIIA) 2023

Member of ACM SIGARCH and IEEE TCCA

Biographical entry in The Marquis Who's Who in the World in the 12th-19th, 24th (2006) editions

Biographical entry in Men of Achievement, the 17th edition (1996)

Biographical entry in The Marquis Who's Who in Finance and Industry (2001)

Biographical entry in The Marquis Who's Who in Science and Engineering (2006-2007)

Became listed on the "IEEE/ACM ISCA Hall of Fame" in 2005 signifying at least eight papers in the IEEE/ACM International Symposium on Computer Architecture Conference series - the most prestigious venues for disseminating research in Computer Architecture.

Became listed on the "IEEE HPCA Hall of Fame" signifying at least six papers in the IEEE International Symposium on High-Performance Computer Architecture Conference series – one of the most prestigious venues for disseminating research in Computer Architecture.

Several HiPEAC Paper awards

HiPEAC Tech. Transfer Award 2016

Member of The Royal Society of Arts and Sciences in Gothenburg, 2017

2020 IEEE TC Award for Editorial Service and Excellence as Topical Editor.

Among the four finalists of supervisors of the year at Chalmers 2021 with an honorary mention.

2021 IEEE TC Award for Editorial Service and Excellence as Topical Editor.

2022 Selected on IVAs 100-list for Research2Business based on EPI and ZeroPoint Innovations

Paper awards:

[1] H. Nilsson and P. Stenstrom: "An Adaptive Update-Based Cache Coherence Protocol for Reduction of Miss Rate and Traffic," *in Proc. of PARLE (Parallel Architectures and Languages Europe)*, pp. 363-374, June 1994. Best Paper Award at the conference.

[2] P. Rundberg and P. Stenstrom: Low-Cost Thread-Level Data Dependence Speculation on Multiprocessors," in *4th Workshop on IEEE Multi-Threaded Execution, Architecture and Compilation (in conj. with Micro-33),* Dec 2000. (Received the Best Paper award.)

[3] H. Dybdahl, P. Stenstrom, L. Natvig, A Cache-Partition Aware Replacement Policy for Chip Multiprocessors. (Best Paper Award.) Accepted to *ACM 2006 HiPC*. December 2006.

[4] F. Warg and P. Stenstrom. Dual-Thread Speculation. Two Threads in the Machine is Better than Eight in the Bush. Accepted to *SBAC 2006*. (Best Paper Award) October 2006

[5] A. Negi, R. Titos, M. Acacio, J.M. Garcia, P. Stenstrom. Pi-TM, HPCA 2012. HiPEAC Award.

[6] A. Arelakis and P. Stenstrom. SC^2 – Statistical Cache Compression Scheme. HiPEAC Award. 2014

[7] A. Arelakis, F. Dahlgren, P. Stenstrom. A Hybrid Cache Compression Method for Selection of Data-Type-Specific Compression Methods. HiPEAC Award 2015

[8] M. Manivannan et al. HiPEAC Award 2016

[9] Knyaginin et al. HiPEAC Award 2018

[10] Angerd et al. HiPEAC Award 2022

[11] Holtryd et al. Nominated for best paper award IEEE HOST 2023

My Mottos (in Swedish and in English)

“Fokusera på vad du verkligen tror på och stå fast vid att skapa det dina tankar ser du kan skapa. De bidrag du då ger kommer inte bara att ge dig själv en stor tillfredsställelse utan kommer att ge ett ännu större bidrag till vårt samhälle.”

In English: “Keep the focus on what you believe in and keep creating what your thoughts envision. Your contributions will not only be rewarding for yourself; they will make a significant contribution to our society.”

Per Stenstrom, October 27, 2010. (Written when I regained energy after the fall of my first startup attempt)

”Det ditt hjärta brinner för ska du alltid prioritera. I detta föds medmänsklighet och ambition att göra världen till en bättre plats för generationer.”

In English: “What your heart says, you should prioritize. From this, compassion and ambition are born to make the world a better place for generations.”

”I allt du gör, sätt etik och medmänsklighet först även om andra i din omgivning inte gör det. I det långa loppet kommer ditt förhållningssätt att vinna och göra världen till en bättre plats för generationer.”

In English: “Make ethics and compassion first-class citizens even if others in your close environment do not do that. Long-term, your perspective will win and make the world a better place for generations.”

Per Stenstrom, September 3, 2018. (Written when having reflected on where I am at this point in my life in my life-long learning process of human life and the wonder about mankind’s ability to do good things and bad things as well.)