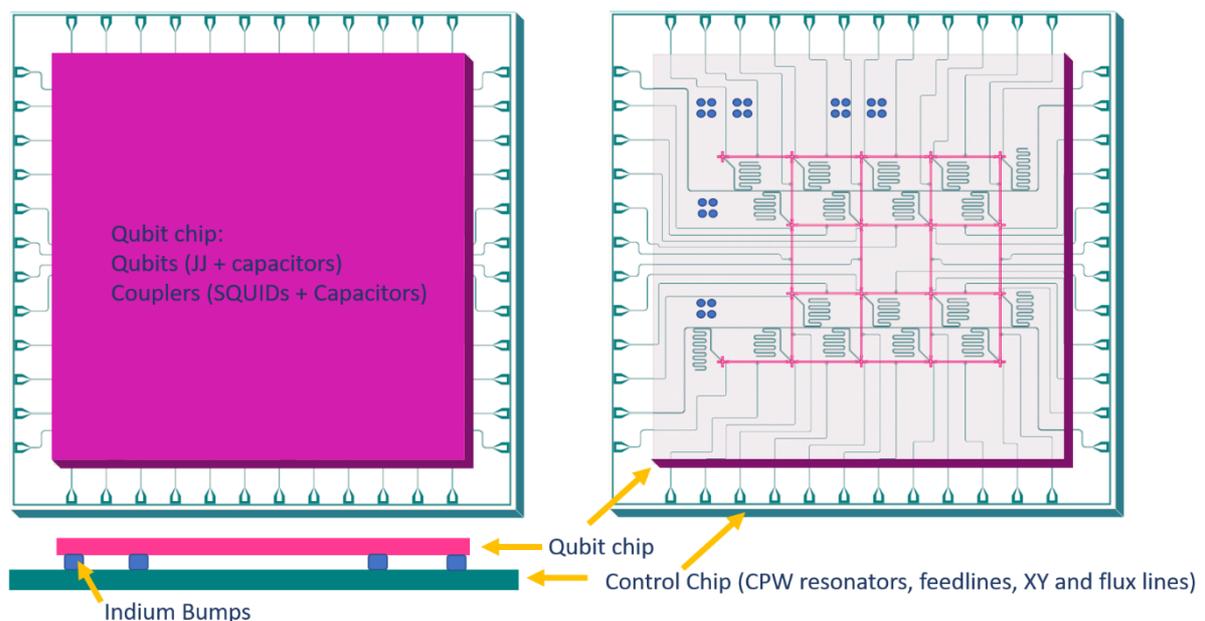


Master's thesis projects co-supervised by the Microwave Electronics and Quantum Technology groups at MC2

PROJECT 3: Design, simulation and fabrication of a controller chip for qubits using Europractice® Circuits Multi-Projects (CMP) (a standard multi-metal layer CMOS process)

Background: Our efforts to scale up the number of qubits in a quantum processor are facing a challenge due to the increased complexity of routing of input/output signals and the footprint of on-chip components. To remedy this, a solution is to use flip-chip technology. In this way, all qubits are fabricated on a separate chip, called the qubit chip (QC), using in-house nano-patterning of aluminum on a silicon substrate. A second, control chip (CC) routes the input/output signals. The control of each qubit requires a microwave pulse (XY line or write line) and a readout resonator (read line). Current research is focused on how to fan out these signals toward the periphery of the chip, whose size is determined by the size of the connectors on the microwave package. This results in a disconnected ground plane, which leads to unwanted resonant modes called slot modes. To avoid this, existing solutions such as air bridges, bond wires, and inter-chip superconducting bumps can stitch the grounds together.

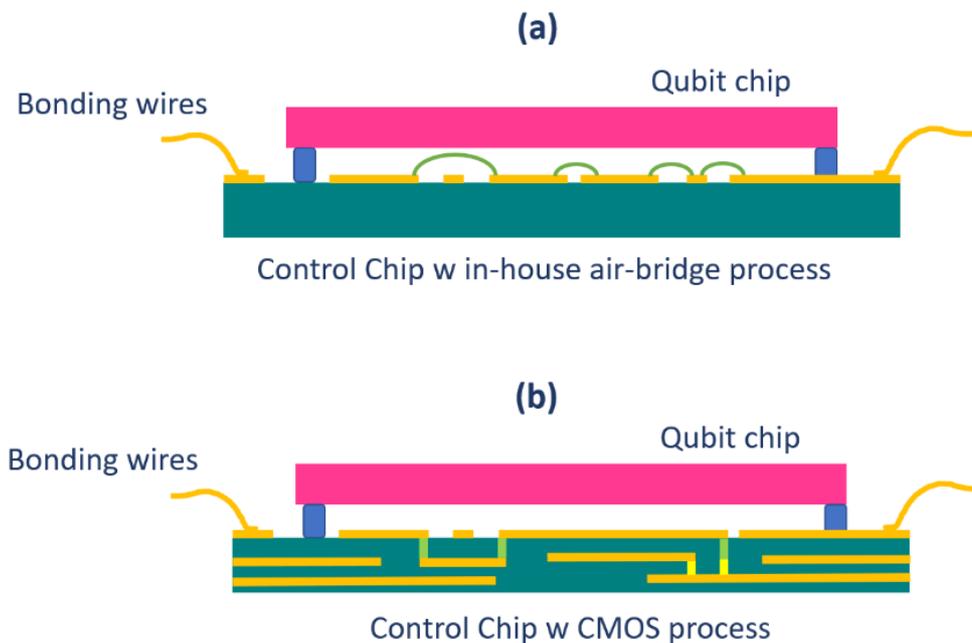
The challenge in this project is that qubits on the QC must have sufficient capacitive coupling to their corresponding read and write lines on the CC. However, the unwanted couplings between different lines and qubits must be mitigated.



Flip-chip solution for an 18-qubit processor. The QC (purple) is composed of cross-shaped capacitors and Josephson junctions (JJ) as qubits. Qubits are coupled capacitively, mediated by a controllable SQUID. All lines to control and read the qubits, e.g. quarter-wavelength resonators, are on the CC (cyan). The lines are connected to the surrounding PCB using wire bonding to the pads on the edge of the chip. There are in total 48 pads for the CC chip that is 14.3 mm X 14.3 mm.

Project Goals: The aim of this project is to use one of the standard semiconductor CMOS processes (without active CMOS devices) to fabricate the control chip and take advantage of the multiple metal layers available in order to route the signal lines on the chip, as well as to avoid crosstalk. Student(s) start learning the design kit purchased from the suitable process provider for CMOS fabrication and flip-chip bonding (e.g. XFAB, ON semiconductor etc.) and install the kit in the industrial chip design and simulation tool Cadence®. The design and floor planning of the control chip for a 20-qubit processor is given to the student(s) to be converted to the chosen design kit (e.g. 4 metal layer CMOS process). The layout design is handed over to colleagues for microwave simulation using e.g. HFSS, and designs are updated based on the simulation results and suggestions. This step may need a few iterations between both parties. The challenges in this part of the project is to think of designing resonators in such a way that the resonators' quality factors do not degrade during the fabrication process. The quality factor of resonators in this process should be investigated and compared with the ones available with our in-house nanolithography e.g. $Q > 10^5 - 10^6$.

The final approved and updated design is sent to the chosen CMOS fabrication and chip bonding service providers. The final flip-chip solution is tested in house and the students(s) can also participate the in the process of testing and measurement should time, budget and interest allow.



(a) The flip-chip module fabricated with in-house nanolithography of Al on Si. The air bridges (in pale green) serve as connecting the overpassing interrupted lines, connecting the split ground planes, and shielding sensitive lines by caging them. In (b), the same design of the control chip (CC) is fabricated using a CMOS process with multi-layer metal to facilitate the routing, grounding and shielding of the sensitive lines using vias (in pale green and yellow).

The student(s) will be helped by senior colleagues who work on fabrication, layout, simulation and cryogenic measurements.

Supervisors: These projects are co-supervised by principal investigators in the Microwave Electronics and Quantum Technology Laboratories a. These projects will contribute to the goal of the Wallenberg Center for Quantum Technologies (WACQT), which is to scale up the size of our quantum processor to 100 qubits. For more information about the activities of both groups consult with the websites, publications or directly contact Professors **Per Delsing, Herbert Zirath, Christian Fager, Jonas Bylander**.

<https://www.chalmers.se/en/centres/wacqt/Pages/default.aspx>

<https://www.chalmers.se/en/departments/mc2/laboratories/MEL/Pages/default.aspx>

For more detailed questions about each project please feel free to contact us or directly ask **Daryoush Shiri** (researcher at QTL) via [shiri@chalmers.se].