Curriculum Vitae

Sally A. McKee

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Research Interests

High-performance/high-efficiency computing; processor, memory systems, and network architecture; performance/power analysis and estimation techniques and tools; power-aware resource management; computer systems modeling; compilers, operating systems, and run-time software.

Education

Ph.D.	Computer Science, University of Virginia, May 1995 "Maximizing Effective Memory Bandwidth for Streamed Computations" Advisor: Wm. A. Wulf
M.S.E.	Computer Science, Princeton University, January 1990
B.A.	Computer Science, Yale University, May 1985

Professional Experience

Chalmers University of Technology, Gothenburg, SE
- 5/16-present Professor, Department of Computer Science and Engineering
- 11/08-5/16 Associate Professor, Department of Computer Science and Engineering

Cornell University, Ithaca, NY, US
- 7/02-11/08 Assistant Professor, School of Electrical and Computer Engineering
- 9/02-11/08 Member, Computer Science Graduate Field of Study

University of Utah, Salt Lake City, UT, US
- 7/02-6/03 Adjunct Assistant Professor, School of Computing
- 9/00-7/01 Research Assistant Professor (joint), Dept.of Electrical Engineering
- 8/98-6/02 Research Assistant Professor, School of Computing

Oregon Graduate Institute of Science and Technology, Portland, OR, US
- 7/96-5/98 Adjunct Assistant Professor, Dept. of Computer Science and Engineering

Intel Corp., Hillsboro, OR, US
- 7/96-5/98 Computer Architect, Microcomputer Research Lab

University of Virginia, Charlottesville, VA, US
- 9/95-5/96 Post Doctoral Research Associate, Department of Computer Science
- 12/91-5/95 Research Assistant, Department of Computer Science

Digital Equipment Corp., Palo Alto, CA, US
- 6/90-8/90 Research Intern, Systems Research Center

AT&T Bell Laboratories, Murray Hill, NJ, US
- 5/88-1/89 Research Intern, Computing Sciences Research Group

Microsoft Corp., Redmond, WA, US
- 3/87-9/87 Software Design Engineer

Digital Equipment Corp., Littleton, MA, US
- 6/85-2/87 Software Engineer II

September 5, 2016

Honors and Awards

HiPEAC Paper Award, "Venice: Exploring server architectures for effective resource sharing at HPCA", J. Dong, R. Hou, M. Huang, T. Jiang, B. Zhao, S.A. McKee, H.Wang, X. Cui, L. Zhang, published in HPCA 2016, award given June 2016.
ACM Service Award (Program Committee co-Chair of Computing Frontiers), May 2014.
ACM Senior Member, 2013
ACM Service Award (General co-Chair of Parallel Architectures and Compilation Techniques), September 2009
IEEE Senior Member, 2007
ACM Service Award (Program Committee Chair of Computing Frontiers), May 2006
IBM Faculty Award, T.J. Watson Research Center, Westchester, NY, 2006
Junior Faculty Fellow, Frontiers in Education Conference, Boulder, CO, November 2003
ACM Service Award (Program Committee co-Chair of Parallel Architectures and Compilation Techniques), September 2002
Best Paper, ACM International Conference on Supercomputing, New York, NY, June 2002
Best Paper, IEEE/ACM International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems, Montreal, QC, July 1998
Graduate Student Award for Excellence, University of Virginia Department of Computer Science, 1994, 1995
Samuel N. Alexander Ph.D. Fellowship, Washington, D.C., ACM Chapter, 1994
Tuition Scholarship for Women, Digital Equipment Corporation, 1990-1992
Graduate Fellowship, University of Virginia Department of Computer Science, 1990-1991
AT&T Bell Laboratories Graduate Fellowship, 1988-1990
John Von Neumann Prize in Supercomputing, Princeton Department of Computer Science, 1987

Funding and Gifts

1. Chinese Academy of Sciences President's International Fellowship Initiative, Visiting Scientist, 280,000 RMB, host: Lixin Zhang, Institute for Computing Technology, CAS, 2015.
2. Vetenskapsrådet (VR), "ACE: Approximate Algorithms and Computing Systems", 9,000,000 SEK, PI P. Stenström, co-PIs U. Assarsson, C. Dimitrakakis, D. Dubhashi, J. Karlsson, S.A. McKee, E. Sintorn, I. Sourdis, 2014.

3.Vetenskapsrådet (VR), "FlexSoft: Software Infrastructure to Support Hardware/Software Co-design of Exposed Architectures", 2,400,000 SEK, PI S.A. McKee, 2012.

4.NVIDIA Corp., Academic Partnership Program, 30 GeForce GTX480 cards, 2011.

5.EC HiPEAC Network of Excellence Compilation Cluster, "Hardware Support for Managed Languages" 12,000€ collaboration grant for travel to interact with Christian Probst, Sven Karlsson (Danish Technical Univ.), 2010. Supplemented by a Danish government grant to include Lixin Zhang (ICT, Beijing) and Michael Franz (UC Irvine).

6. EC 7th Framework Programme 249059, "Embedded Reconfigurable Architectures", Chalmers portion 256,332€, main PI S. Wong, co-PIs from Delft, Uppsala, Siena, Edinburgh, Federal Univ. of the Rio Grande do Sul, Evidence, ST Microelectronics, IBM Israel, 2010.
7. Ericsson AB, "Smarter Resource Management for Baseband Processing", 880,000 SEK, PI S.A. McKee, 2009; extension 250,000 SEK, 2011.
8. Vetenskapsrådet (VR), "Chalmers Adaptive Multicore Processing Project (CHAMPP)", Co-PIs P. Stenström, P. Lars-Edefors, S.A. McKee, L.J. Svensson, 11,142,000 SEK, 2009.
9. EC HiPEAC Network of Excellence Adaptive Compilation Cluster, 10,000€ collaborative grant for travel to University of Siena, PI S.A. McKee, 2008.

10. NSF 0750851 “CRI: CRD Collaborative Research: Archer — Seeding a Community-Based Computing Infrastructure for Computer Architecture Research and Education”, main PI R.J.O. Figueiredo, co-PIs from Univ. of Florida, Florida State Univ., Univ. of Texas at Austin, Northeastern Univ., Univ. of Minnesota, Northwestern Univ., 2007.
11. DOE Lawrence Livermore National Laboratory Center for Applied Scientific Computing subcontract B571234, PI D. Quinlan; “Leveraging OpenAnalysis for Alias Analysis within ROSE”, PI S.A. McKee, $40,000, 2007.
12. NSF CNS Award 0708788, “CRI: IAD Keeping Pace with Growing Computing Needs: A Strategy for Enhancing Multi-Core Microprocessor Research and Education at Cornell University”, co-PIs D. Albonesi, J.F. Martínez, S.A. McKee, $93,865, 2007.
13. NSF CCF Award 0702616, “Towards Designing Complex Systems: Exponential Design/Configuration/Parameter Space Exploration Tools That Are Efficient, Accurate, and Easily Usable”, PI S.A. McKee, $300,000, 2007-2010.
14. Intel Academic Equipment Donations (components for a 64-bit Xeon cluster), $26,030, 2007.
15. Intel Academic Equipment Donations (six Dell laptops for undergraduate research “mobile lab”), PI S.A. McKee, 2006.
16. Intel Research Foundation Equipment Donation (120 dual-processor 64-bit x86 chips), PI S.A. McKee, 2006.
17. NSF CNS Award 0509406, “Collaborative SMA: Dynamic Program Phase Adaptation and Hardware Reconfiguration in Multiprocessor Systems”, PI J.F. Martínez, Co-PI S.A. McKee, $350,000 total, $150,000 to PI McKee, 2005-2007.
18. Intel Research Foundation Equipment Donation, PI S.A. McKee, $74,374, 2004-2005.
19. DOE Lawrence Livermore National Laboratory Center for Applied Scientific Computing award, ASC, PI D. Dossa; “BlueGene/L: Studies in Scalability and Reconfigurability: Memory Performance”, Subcontract PI S.A. McKee, $65,000, 2004-2005.
20. Intel Academic Equipment Donation, PI S.A. McKee, $67,413, 2004.
21. NSF ST-HEC Award 0444413, “Scalable, Interoperable Tools to Support Autonomic Optimization of High-End Applications”, Main PI S.A. McKee, co-PIs A. Malony (University of Oregon) and G.S. Tyson (University of Florida) $750,000 (PI McKee amount $329,670), 2004-2007.
22. REU Supplement 0530488 to award NSF ST-HEC Award 0444413, PI S.A. McKee, $15,000, 2004.
23. NSF ITR/NGS Medium Award 0325536, “Toward Autonomous Computing: System-Wide Hardware/Software Monitoring and Adaptation”, Main PI S.A. McKee, co-PI H.S. Lee (Georgia Institute of Technology), $830,000 (PI McKee amount $415,000), 2003-2008.
24. REU Supplement 0434682 to NSF ITR/NGS Medium Award 0325536, PI S.A. McKee, $12,000, 2004.
25. Cornell University, President’s Council of Cornell Women Affinito-Stewart Junior Faculty Award, PI S.A. McKee, $9,500, 2003.
26. AAAS/NSF Women’s International Science Cooperation Travel Grant, with Universitat Politècnica de Catalunya, PI S.A. McKee, $4,000, 2003.
27. Cornell University, Cornell Information Technology Innovation in Teaching Grant, PI S.A. McKee, 2003-2004.
28. Small Business Initiative for Research (SBIR) Award, PIs: SRC Computers, Inc., $15,000, Subcontract PI S.A. McKee, 2002.
29. DOE Lawrence Livermore National Laboratory Center for Applied Scientific Computing award LLNL LDRD 01-ERD-043, PI B.R. de Supinski; collaborator: A. Yoo; “Overcoming the Memory Wall for SMP-Based Systems”. Subcontract PI S.A. McKee, $238,000, 2001.

30. Intel Foundation Equipment Donation, "The Impulse Memory Controller Project", PI S.A. McKee, co-PI J.B. Carter, $10,000, 2001.
31. NSF CCR CSA Award 0073532, "Understanding and Improving Memory System Performance", $184,998, PI S.A. McKee, 2000-2003.
32. REU Supplement 0211668 to NSF CCR CSA Award 0073532, PI S.A. McKee, $5,000, 2002.
33. CRA Distributed Mentor Program, support for three interns, summers 1999, 2000.
34. NSF POWRE Award 9806043, "Understanding and Improving Memory System Performance", PI S.A. McKee, $75,000, 1998-2000.

Publications and Patents (h-index 29, i10-index 66 — Google Scholar Citations, September 2016)

Patents

1 . Wm.A. Wulf, S.A. McKee, R.H. Klenke, A.J. Schwab, S.A. Moyer, J.H. Aylor, C.Y. Hitchcock, III, "Method and Device for Maximizing Memory System Bandwidth by Accessing Data in a Dynamically Determined Order"; U.S. Patent 6,154,826. November 28, 2000.

Books

2. S.A. McKee, "Maximizing Memory Bandwidth for Streamed Computations", Ph.D. Dissertation, University of Virginia, May 1995.

Book Chapters

3. B. Goel, S.A. McKee, M. Själander, "Techniques to Measure, Model, and Manage Power", Elsevier Advances in Computers, vol. 87, *Green Computing*, November 2012, pp. 7-54.
4. S. Wong, L. Carro, M. Rutzig, M.M. Matos, R. Giorgi, N. Puzovic, S. Kaxiras, M. Cintra, G. Desoli, P. Gai, S.A. McKee, A. Zaks, "ERA — Embedded Reconfigurable Architectures", *Reconfigurable Computing: From FPGAs to Hardware/Software Co-design*, J.M.P. Cardoso, M. Hübner, Eds., Springer, July 2011, pp. 239-259.
5. S.A. McKee, R.W. Wisniewski, "The Memory Wall", *Encyclopedia of Parallel Computing*, D. Padua, Ed., Springer, 2011, pp. 1110-1116.

Refereed Journals

6. T. Jiang, R. Hou, J. Dong, L. Chai, S.A. McKee, B. Tian, L. Zhang, N. Sun, "Adapting Memory Hierarchies for Emerging Datacenter Interconnects", *Springer Journal of Computer Science and Technology*, 30(1):97–109, January 2015. DOI 10.1007/s11390-015-1507-4.
7. Z. Fang, L. Zhang, J.B. Carter, S.A. McKee, X. Jiang, A. Ibrahim, M.A. Parker, "Active Memory Controllers", *Springer Journal of Supercomputing*, 62(1):510-549, October 2012.
8. M. Bhadauria, S.A. McKee, K. Singh, G.S. Tyson, "Data Cache Techniques to Save Power and Deliver High Performance in Embedded Systems", *Transactions on High Performance Embedded Architectures and Compilers II*, 2(1):65-84, Springer LNCS 5470, 2009.
9. N. Xu, S.A. McKee, L. Nozick, R. Ufomata, "Augmenting Priority Rule Heuristics with Justification and Rollout to Solve the Resource-Constrained Project Scheduling Problem", *Elsevier Computers and Operations Research*, 35(10):3284-3297, October 2008.
10. K. Singh, E. Ipek, S.A. McKee, B.R. de Supinski, M. Schulz, R. Caruana, "Predicting Parallel Application Performance via Machine Learning Approaches", *Wiley Concurrency and Computation: Practice and Experience*, 19(17):2219-2235, May 2008.
11. E. Ipek, S.A. McKee, K. Singh, R. Caruana, B.R. de Supinski, M. Schulz, "Efficient Architectural Design Space Exploration via Predictive Modeling", *ACM Transactions on Architecture and Code Optimization*, 4(4), Article 1, January 2008.

12. J. Marathe, F. Mueller, T. Mohan, S.A. McKee, B.R. de Supinski, A. Yoo, "METRIC: Memory Tracing via Dynamic Binary Rewriting to Identify Cache Inefficiencies", *ACM Transactions on Programming Languages and Systems,* 29(2), Article 12, April 2007.
13. M.J. Geiger, S.A. McKee, G.S. Tyson, "Specializing Cache Structures for High Performance and Energy Conservation in Embedded Systems", *Transactions on High Performance Embedded Architectures and Compilers*, 1(1):50-90, January 2007.
14. A. Bunker, G. Gopalakrishnan, S.A. McKee, "Formal Hardware Specification Languages for Protocol Compliance Verification", *ACM Transactions on Design Automation of Electronic Systems*, 9(1):1-32, January 2004.
15. B. Chandramouli, W.C. Hsieh, J.B. Carter, S.A. McKee, "A Cost Model for Integrated Restructuring Optimizations", *Journal of Instruction Level Parallelism*, Volume 5, paper 9, August 2003.
16. V.S. Pingali, S.A. McKee, W.C. Hsieh, J.B. Carter, "Restructuring Computations for Temporal Data Cache Locality", Springer *International Journal of Parallel Programming*, 31(4):305-338, August 2003.
17. L. Zhang, Z. Fang, M. Parker, B.K. Mathew, L. Schaelicke, J.B. Carter, W.C. Hsieh, S.A. McKee, "The Impulse Memory Controller", *IEEE Transactions on Computers*, 50(11):1117-1132, November 2001.
18. S.A. McKee, Wm.A. Wulf, J.H. Aylor, R.H. Klenke, M.H. Salinas, S.I. Hong, D.A.B. Weikle, "Dynamic Access Ordering for Streamed Computations", *IEEE Transactions on Computers*, 49(11):1255-1271, November 2000.
19. J.B. Carter, W.C. Hsieh, L.B. Stoller, M.R. Swanson, L. Zhang, S.A. McKee, "Impulse: Memory System Support for Scientific Applications", *IOS Scientific Programming*, 7(3-4):195-209, fall 1999.
20. S.A. McKee, R.H. Klenke, M.H. Salinas, K.L. Wright, Wm.A. Wulf, J.H. Aylor, A.P. Batson, "Smarter Memory: Improving Memory Bandwidth for Streamed References", *IEEE Computer*, 31(7):54-63, July 1998.

Refereed Conferences

21. C. Sanchez, P. Gavin, D. Moreau, M. Själander, D. Whalley, P. Larsson-Edefors, S.A. McKee, "Redesigning a Tagless Access Buffer That Requires Minimal ISA Changes", ACM/IEEE International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), October 2016.
22. Y. Chang, K. Zhang, S.A. McKee, L. Zhang, M. Chen, L. Ren and Z. Xu, "Extending On-Chip Server Node Interconnections for Rack-Level Remote Resource Access", IEEE International Conference on Computer Design (ICCD), October 2016 (29% acceptance).
23. K. Zhang, L. Yu, Y. Chang, R. Zhao, H. Zhang, L. Zhang, M. Chen, S.A. McKee, "Co-DIMM Inter-Socket Data Sharing via a Common DIMM Channel", International Conference on Memory Systems (MEMSYS), October 2016, pp. 135-143.
24. Z. Cui, T. Luy, S.A. McKee, M. Chen, H. Pan, Y. Ruan, "Twin-Load: Bridging the Gap between Conventional Direct-Attached and Buffer-on-Board Memory Systems", International Conference on Memory Systems (MEMSYS), October 2016, pp. 166-178.
25. L. Zhang, R. Hou, S.A. McKee, J. Dong, L. Zhang, "P-Socket: Optimizing a Communication Library for a PCIe-Based Intra-Rack Interconnect", ACM Conference on Computing Frontiers (CF), May 2016, pp. 145-153 (26% acceptance).

26. B. Goel, S.A. McKee, “A Methodology for Modeling Dynamic and Static Power Consumption”, IEEE International Parallel and Distributed Processing Symposium (IPDPS), May 2016, pp. 273-282 (23% acceptance).
27. M. Brown, Z. Yannes, M. Sanati, M. Lustig, S.A. McKee, G.S. Tyson, S.K. Reinhardt, “Agave: a Benchmark Suite for Exploring the Complexities of the Android Software Stack”, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), April 2016 (abstract/poster).
28. J. Dong, R. Hou, M. Huang, T. Jiang, B. Zhao, S.A. McKee, H.Wang, X. Cui, L. Zhang, “Venice: Exploring Server Architectures for Effective Resource Sharing”, IEEE High Performance Computer Architecture (HPCA), March 2016, pp. 507-518 (industry session).
29. W. Wei, D. Jiang, S.A. McKee, J. Xiong. M. Chen, “Exploiting Program Semantics to Place Data in Hybrid Memory”, ACM/IEEE/IFIP Parallel Architectures and Compilation Techniques (PACT), October 2015, pp. 163-173 (21% acceptance).
30. M. Radulovic, D. Zivanovic, D. Ruiz, B.R. de Supinski, S.A. McKee, P. Radojkoviç, E. Ayguadé, “Another Trip to the Wall: How Much Will Stacked DRAM Benefit HPC?”, MEMSYS, October 2015, pp. 31-36.
31. T. Jiang, Q. Zhang, R. Hui, L. Chai, S.A. McKee, Z. Jia, N. Sun, “Understanding the Behavior of in-Memory Computing Workloads”, IEEE International Symposium on Workload Characterization (IISWC), October 2014, pp. 22-30 (27.5% acceptance).
32. Z. Jia, J. Zhan, L. Wang, R. Han, S.A. McKee, “Characterizing and Subsetting Big Data Workloads”, IEEE International Symposium on Workload Characterization (IISWC), October 2014 pp. 191-201 (27.5% acceptance).
33. X. Fu, S.A. McKee, J. Zhan, “Digging Deeper into Cluster System Logs for Failure Prediction and Root Cause Diagnosis”, IEEE International Conference on Cluster Computing (Cluster), September 2014, pp. 103-112 (23.8% acceptance).
34. Z. Cui, S.A. McKee, Z. Zha, Y. Bao, M. Chen, “DTail: A Flexible Approach to DRAM Refresh Management”, ACM International Conference on Supercomputing (ICS), June 2014, pp. 43-52 (21% acceptance).
35. Z. Yao, X. Sui, T. Xu, J. Ma, J. Fang, S.A. McKee, B. Fu, Y. Bao, “QBLESS: A Case for QoS-Aware Bufferless NoCs”, International Symposium on Quality of Service (IWQoS), May 2014, pp. 93-98.
36. B. Goel, R. Titos-Gil, A. Negi, S.A. McKee, P. Stenström, “Performance and Energy Analysis of the Restricted Transactional Memory Implementation on Haswell”, IEEE International Parallel and Distributed Processing Symposium (IPDPS), May 2014, pp. 615-624 (21% acceptance).
37. G. Keramidas, S. Wong, F. Anjam, A. Brandon, R. Seedorf, C. Scordino, L. Carro, D. Matos, R. Giorgi, S. Kavvadias, S.A. McKee, B. Goel, V. Spiliopoulos, “Embedded Reconfigurable Computing: the ERA Approach”, IEEE International Conference on Industrial Informatics (INDIN), July 2013, pp. 827-832.
38. A. Bardizbanyan, P. Gavin, M. Själander, D. Whalley, S.A. McKee, P. Stenström, P. Larsson-Edefors, “Improving Data Access Efficiency by Using a Tagless Access Buffer (TAB)”, ACM/IEEE International Symposium on Code Generation and Optimization (CGO), February 2013, pp. 269-279 (28% acceptance).
39. P. Larsen, R. Ladelsky, J. Lidman, S.A. McKee, S. Karlsson, A. Zaks, “Parallelizing More Loops with Compiler Guided Refactoring”, International Conference on Parallel Processing (ICPP), September 2012, pp. 410-419 (28.3% acceptance).

40. M. Själander, S.A. McKee, P. Brauer, D. Engdal, A. Vajda, “An LTE Uplink Receiver PHY Benchmark and Subframe-Based Power Management”, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), April 2012, pp. 25-34 (48% acceptance; nominated for best paper award).
41. P. Schleuniger, S.A. McKee, S. Karlsson, “Design Principles for Synthesizable Processor Cores”, International Conference on Architecture of Computing Systems (ARCS), February 2012, pp. 111-122 (31% acceptance).
42. M. Gschwind, V. Salapura, C. Trammell, S.A. McKee, “SoftBeam: Precise Tracking of Transient Faults and Vulnerability Analysis at Processor Design Time”, IEEE International Conference on Computer Design (ICCD), October 2011, pp. 404-410 (28% acceptance).
43. M. Själander, S.A. McKee, B. Goel, P. Brauer, D. Engdal, A. Vajda, “Power Aware Resource Scheduling in Base Stations”, IEEE International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS), July 2011, pp. 462-465.
44. S. Wong, A. Brandon, F. Anjam, R. Seedorf, R. Giorgi, Z. Yu, N. Puzovic, S.A. McKee, M. Själander, G. Keramidas, L. Carro, “Early Results from ERA — Embedded Reconfigurable Architectures”, IEEE International Conference on Industrial Informatics (INDIN), July 2011.
45. J. Wiedendorfer, T. Küstner, S.A. McKee, “Performance Optimization by Dynamic Code Transformation”, ACM Conference on Computing Frontiers (CF), May 2011 (short paper).
46. J. Lidman, S.A. McKee, “Increasing Opportunities for Automatic Parallelization”, ACM Conference on Code Generation and Optimization (CGO), April 2011 (abstract/poster).
47. P. Larsen, R. Ladelsky, J. Lidman, S.A. McKee, S. Karlsson, A. Zaks, “Interactive Compilation and Code Modification to Automatically Parallelize Loops”, ACM/IEEE Conference on Code Generation and Optimization (CGO), April 2011 (abstract/poster).
48. N. Puzovic, S.A. McKee, R. Eres, A. Zaks, P. Gai, S. Wong, R. Giorgi, “A Multi-Pronged Approach to Benchmark Characterization”, IEEE International Conference on Cluster Computing (CLUSTER), September 2010 (short paper/poster).
49. R. Gioiosa, S.A. McKee, M. Valero, “Designing an OS for HPC: Scheduling”, IEEE International Conference on Cluster Computing (CLUSTER), September 2010, pp. 78-87 (31% acceptance).
50. K. Singh, M. Curtis-Maury, S.A. McKee, F. Blagojevic, D.S. Nikolopoulos, B.R. de Supinski, M. Schulz, “Comparing Scalability Prediction Strategies on an SMP of CMPs”, Euro-Par, September 2010, pp. 143-155 (35% acceptance).
51. B. Goel, S.A. McKee, R. Gioiosa, K. Singh, M. Bhadauria, M. Cesati, “Portable per-Core Power Estimation for Intelligent Resource Management”, IEEE International Green Computing Conference (IGCC), August 2010.
52. M. Bhadauria, S.A. McKee, “An Approach to Resource-Aware co-Scheduling for CMPs”, ACM International Conference on Supercomputing (ICS), June 2010, pp. 189-199 (18% acceptance).
53. M. Zahran, S.A. McKee, “Global Management of Cache Hierarchies”, ACM Conference on Computing Frontiers (CF), May 2010, pp. 131-140 (27% acceptance).
54. V.M. Weaver, S.A. McKee, “Code Density Concerns for New Architectures”, IEEE International Conference on Computer Design (ICCD), October 2009, pp. 459-464 (34% acceptance).

55. M. Bhadauria, V.M. Weaver, S.A. McKee, "Understanding PARSEC Performance on Contemporary CMPs", IEEE International Symposium on Workload Characterization (IISWC), October 2009, pp. 98-107 (41% acceptance).
56. K. Singh, M. Bhadauria, S.A. McKee, "Prediction-Based Power Estimation and Scheduling for CMPs", ACM International Conference on Supercomputing (ICS), June 2009, pp. 501-502 (abstract/poster).
57. M. Bhadauria, V. Weaver, S.A. McKee, "PARSEC: Hardware Profiling for CMP Design of Emerging Workloads", ACM International Conference on Supercomputing (ICS), June 2009, pp. 509-510 (abstract/poster).
58. Md. Mafijul Islam, P. Stenström, S.A. McKee, "Cancellation of Loads that Return Zero Using Zero Valued Caches", ACM International Conference on Supercomputing (ICS), June 2009, pp. 493-494 (abstract/poster).
59. P.E. West, Y. Peress, G.S. Tyson, S.A. McKee, "Core Monitors: Monitoring Performance in Multicore Processors", ACM Conference on Computing Frontiers (CF), May 2009, pp. 31-40 (23% acceptance).
60. G. Bronevetsky, K. Pingali, D. Marques, R. Rugina, S.A. McKee, "Compiler-Enhanced Incremental Checkpointing for OpenMP Applications", International Parallel and Distributed Processing Symposium (IPDPS), May 2009, pp.1-12 (23% acceptance).
61. J. Li, X. Ma, K. Singh, M. Schulz, B.R. de Supinski, S.A. McKee, "Machine Learning Based Online Performance Prediction for Runtime Parallelization and Task Scheduling", IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), April 2009, pp. 89-100 (28% acceptance).
62. V.M. Weaver, S.A. McKee. "Optimizing for Size: Exploring the Limits of Code Density", ACM/IEEE Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2009 (poster).
63. G. Venkatasubramanian, D. Wolinsky, R.J.O. Figueiredo, P.O. Boykin, J.A.B. Fortes, T. Li, J.-K. Peir, L.K. John, D. Kaeli, D. Lilja, S.A. McKee, G. Memik, A. Roy, B. Burnett, G.S. Tyson, "A Community Distributed Infrastructure for Computer Architecture Research and Education", ACM/IEEE Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2009 (poster).
64. M. Bhadauria, V.M. Weaver, S.A. McKee, "Accommodating Diversity in CMPs with Heterogeneous Frequencies", International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), January 2009, pp. 248-262 (28% acceptance).
65. M.A. Watkins, S.A. McKee, L. Schaelicke, "Revisiting Cache Block Superloading: A Phase-Adaptive Approach to Increasing Cache Performance", International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), January 2009, pp. 339-354 (28% acceptance).
66. R.J.O. Figueiredo, P.O. Boykin, J.A.B. Fortes, T. Li, J.-K. Peir, D. Wolinsky, L.K. John, D.R. Kaeli, D.J. Lilja, S.A. McKee, G. Memik, A. Roy, G.S. Tyson, "Archer: A Community Distributed Computing Infrastructure for Computer Architecture Research and Education", International Conference on Collaborative Computing: Networking, Applications and Worksharing (CollaborateCom), November 2008, pp. 70-84.
67. V.M. Weaver, S.A. McKee, "Can Hardware Performance Counters be Trusted?", IEEE International Symposium on Workload Characterization (IISWC), September 2008, pp. 141-150 (35% acceptance).

68. B.S. White, S.A. McKee, D.J. Quinlan, "A Projection-Based Optimization Framework for Abstractions with Application to the Unstructured Mesh Domain", ACM International Conference on Supercomputing (ICS), June 2008, pp.104-113 (30% acceptance).
69. P.A. Castillo, A.M. Mora, J.J. Merelo, J.L.J. Laredo, M. Moreto, F.J. Cazorla, M. Valero, S.A. McKee, "Evolutionary System for Prediction and Optimization of Hardware Architecture Performance", IEEE Congress on Evolutionary Computation (CEC), May 2008, pp. 1941-1948.
70. M. Bhadauria, S.A. McKee, "Optimizing Thread Throughput for Multithreaded Workloads on Memory Constrained CMPs", ACM Computing Frontiers (CF), May 2008.
71. G. Bronevetsky, D. Marques, K. Pingali, S.A. McKee, R. Rugina, "Compiler-Enhanced Incremental Checkpointing for OpenMP Applications", ACM Symposium on Principles and Practices of Parallel Programming (PPoPP), February 2008, pp. 275-276 (abstract/poster).
72. V.M. Weaver, S.A. McKee, "Using Dynamic Binary Instrumentation to Generate Multi-Platform SimPoints: Methodology and Accuracy", International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), January 2008, pp. 305-319 (34% acceptance).
73. M. Watkins, S.A. McKee, L. Schaelicke, "A Phase Adaptive Approach to Increasing Cache Performance", ACM/IEEE/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT), September 2007 (abstract/poster).
74. C. Dolen, C. Haymes, K. Inoue, D. Kuchta, S. Lekuch, J.E. Moreira, E. Shenfield, X. Shen, C. Trammell, M. Tsao, S.A. McKee, "Chameleon Shared Memory Project", 8th Linux Cluster Institute International Conference on High-Performance Clustered Computing (LCI), May 2007 (best poster).
75. B.C. Lee, D.M. Brooks, B.R. de Supinski, M. Schulz, K. Singh, S.A. McKee, "Methods of Inference and Learning for Performance Modeling of Parallel Applications", ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP), March 2007, pp. 240-258 (33% acceptance).
76. M. Bhadauria, S.A. McKee, K. Singh, G.S. Tyson, "Leveraging High Performance Data Cache Techniques to Save Power in Embedded Systems", International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), February 2007, pp. 23-37 (29% acceptance).
77. N.B. Sam, S.A. McKee, P. Kudva, "Rethinking Processor Design: Parameter Correlations", IEEE International Conference on Electronics, Circuits and Systems (ICECS), December 2006, pp. 156-159 (62% acceptance).
78. E. Ipek, S.A. McKee, B.R. de Supinski, M. Schulz, R. Caruana, "Efficiently Exploring Architectural Design Spaces via Predictive Modeling", ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), October 2006, pp. 195-206 (24% acceptance).
79. M. Bhadauria, S.A. McKee, K. Singh, G.S. Tyson, "A Precisely Tunable Drowsy Cache Management Mechanism", 3rd IBM P=ac2 (P= Power/Performance, a=architecture, c2=circuit*compilers) Conference, October 2006 (33% acceptance).
80. M.J. Geiger, S.A. McKee, G.S. Tyson, "Beyond Region Caching: Specializing Cache Structures for High Performance and Energy Conservation", International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), November 2005, pp. 102-115 (20% acceptance).
81. E. Ipek, B.R. de Supinski, M. Schulz, S.A. McKee, "An Approach to Performance Prediction for Parallel Applications", Euro-Par, August 2005, pp. 196-205 (30% acceptance).

82. B.S. White, S.A. McKee, B.R. de Supinski, B.J. Miller, D.J. Quinlan, M. Schulz, "Improving the Computational Intensity of Unstructured Grid Applications", ACM International Conference on Supercomputing (ICS), June 2005, pp. 341-350 (28% acceptance).
83. M.J. Geiger, S.A. McKee, G.S. Tyson, "Drowsy Region-Based Caches: Minimizing Both Dynamic and Static Power Dissipation", ACM International Conference on Computing Frontiers (CF), May 2005, pp. 378-384 (acceptance 41%).
84. M. Schulz, B.S. White, S.A. McKee, H.S. Lee, J. Jeitner, "Owl: Next-Generation System Monitoring", ACM International Conference on Computing Frontiers (CF), May 2005, pp. 116-124 (acceptance 41%).
85. S.A. McKee, "Reflections on the Memory Wall", ACM International Conference on Computing Frontiers (CF), April 2004, pp. 162-167 (invited paper).
86. T. Mohan, B.R. de Supinski, S.A. McKee, F. Mueller, A. Yoo, M. Schulz, "Identifying and Exploiting Spatial Regularity in Data Memory References", ACM/IEEE Supercomputing: International Conference on High Performance Computing, Networking, Storage, and Analysis (SC), November 2003, p. 49 (29% acceptance).
87. S.A. McKee, D.M. Kubarek, "Real World Engineering: a Course for Masters Students Headed for Industry", ASEE/IEEE Frontiers in Education Conference (FIE), November 2003, Session F1E, pp. 16-21.
88. T. Mu, J. Tao, M. Schulz, S.A. McKee, "Interactive Locality Optimization on NUMA Architectures", ACM Symposium on Software Visualization (SoftVis), June 2003, pp. 133-142 (31% acceptance).
89. M. Schulz, S.A. McKee, "A Framework for Portable Shared-Memory Programming", IEEE/ACM International Parallel and Distributed Processing Symposium (IPDPS), April 2003, pp. 54-62 (29% acceptance).
90. J. Marathe, F. Mueller, T. Mohan, B.R. de Supinski. S.A. McKee, A. Yoo, "METRIC: Tracking Down Inefficiencies in the Memory Hierarchy via Binary Rewriting", ACM/IEEE International Symposium on Code Generation and Optimization (CGO), March 2003, pp. 289-300 (35% acceptance).
91. Z. Fang, S.A. McKee, M. Valero, "An MPEG-4 Performance Study", IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), March 2003, pp. 49-57 (33% acceptance).
92. M. Tao, J. Tao, M. Schulz, S.A. McKee, "Visualizing Data Distribution on NUMA Architectures to Guide Incremental Optimizations", ACM/IEEE Supercomputing: International Conference on High Performance Computing, Networking, Storage, and Analysis (SC), November 2002 (poster).
93. A. Bunker, S.A. McKee, G. Gopalakrishnan, "An Overview of Formal Hardware Specification Languages", Grace Hopper Celebration of Women in Computing (GHC), October 2002.
94. V.K. Pingali, S.A. McKee, W.C. Hsieh, J.B. Carter, "Computation Regrouping: Restructuring Programs for Temporal Data Cache Locality", ACM International Conference on Supercomputing (ICS), June 2002, pp. 252-261 (PC-voted best paper award, 20% acceptance).
95. B. Chandramouli, J.B. Carter, W.C. Hsieh, S.A. McKee, "A Cost Framework for Evaluating Integrated Restructuring Optimizations", ACM/IEEE/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT), September 2001, pp. 131-140 (21% acceptance).

96. Z. Fang, L. Zhang, J.B. Carter, S.A. McKee, W.C. Hsieh, "Reevaluating Online Superpage Promotion with Hardware Support", IEEE Symposium on High Performance Computer Architecture (HPCA), January 2001, pp. 63-72 (24% acceptance).
97. D.A.B. Weikle, S.A. McKee, K. Skadron, Wm.A. Wulf, "Caches as Filters: a Framework for the Analysis of Caching Systems", Grace Hopper Celebration of Women in Computing (GHC), September 2000.
98. L. Schaelicke, A. Davis, S.A. McKee, "Profiling Interrupts in Modern Architectures", 8th IEEE International Symposium on Modeling, Analysis and Simulation of Computers and Telecommunication Systems (MASCOTS), August 2000, pp. 115-123.
99. B.K. Mathew, S.A. McKee, J.B. Carter, A. Davis, "Algorithmic Foundations for a Parallel Vector Access Memory System", ACM Symposium on Parallel Algorithms and Architectures (SPAA), July 2000, pp. 156-165 (29% acceptance).
100. Z. Fang, L. Zhang, S.A. McKee, J.B. Carter, W.C. Hsieh, "Online Superpage Promotion Revisited", ACM International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS), June 2000, pp. 114-115 (.).
101. C. Zhang, S.A. McKee, "Hardware-Only Stream Prefetching and Dynamic Access Ordering", ACM International Conference on Supercomputing (ICS), May 2000, pp. 167-175 (27% acceptance).
102. B.K. Mathew, S.A. McKee, J.B. Carter, A. Davis, "Design of a Parallel Vector Access Unit", IEEE International Symposium on High Performance Computer Architecture (HPCA), January 2000, pp. 39-48 (21% acceptance).
103. L. Zhang, J.B. Carter, W.C. Hsieh, S.A. McKee, "Memory System Support for Image Processing", IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT), October 1999, pp. 98-107 (21% acceptance).
104. S.I. Hong, S.A. McKee, M.H. Salinas, R.H. Klenke, J.H. Aylor, Wm.A. Wulf, "Access Order and Effective Bandwidth for Streams on a Direct Rambus Memory", IEEE International Symposium on High Performance Computer Architecture (HPCA), January 1999, pp. 80-89 (21% acceptance).
105. D.A.B. Weikle, S.A. McKee, Wm.A. Wulf, "Caches as Filters: A New Approach to Memory Hierarchy Analysis", IEEE International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS), July 1998, pp.1-11 (best paper award).
106. S.A. McKee, C.W. Oliver, Wm.A. Wulf, K.L. Wright, J.H. Aylor, "Design and Evaluation of Dynamic Access Ordering Hardware", ACM International Conference on Supercomputing (ICS), May 1996, pp. 125-132 (43% acceptance).
107. S.A. McKee, Wm.A. Wulf, "A Memory Controller for Improved Performance of Streamed Computations on Symmetric Multiprocessors", IEEE/ACM International Parallel Processing Symposium (IPPS), April 1996, pp. 159-165 (36% acceptance).
108. S.A. McKee, S.A. Moyer, Wm.A. Wulf, C.Y. Hitchcock, "Bounds on Memory Bandwidth in Streamed Computations", Euro-Par, September 1995, pp. 83-99 (27% acceptance).
109. T.C. Landon, R.H. Klenke, J.H. Aylor, M.H. Salinas, S.A. McKee, "An Approach for Optimizing Synthesized High-Speed ASICs", IEEE International ASIC Conference on Application Specific Integrated Circuits (ASIC), September 1995, pp. 245-248 (31% acceptance).
110. S.A. McKee, Wm.A. Wulf, "Access Ordering and Memory-Conscious Cache Utilization", IEEE Symposium on High Performance Computer Architecture (HPCA), January 1995, pp. 253-262 (19% acceptance).

111. S.A. McKee, S.A. Moyer, Wm.A. Wulf, C. Hitchcock, "Increasing Memory Bandwidth for Vector Computations", International Conference on Programming Languages and System Architectures (PLSA), March 1994, pp. 87-104.
112. S.A. McKee, R.H. Klenke, A.J. Schwab, Wm.A. Wulf, S.A. Moyer, C. Hitchcock, J.H. Aylor, "Experimental Implementation of Dynamic Access Ordering", Hawaii International Conference on Systems Sciences (HICSS), January 1994, pp. 431-440.
113. T. Barrera, J. Griffith, S.A. McKee, G. Robins, T. Zhang, "Toward a Steiner Engine: Enhanced Serial and Parallel Implementations of the Iterated 1-Steiner MRST Algorithm", Great Lakes Symposium on VLSI (GLS-VLSI), March 1993, pp. 90-94.

Refereed Workshops

114. O. Jeppsson, S.A. McKee, "Towards a Scalable Functional Simulator for the Adapteva Epiphany Architecture", Workshop on Programmability for Multicores (MULTIPROG), January 2015.
115. O. Jeppsson, S.A. McKee, "Simulating a Manycore Processor: A Scalable Functional Model for the Adapteva Epiphany Architecture", Swedish Workshop on Multicore Computing (MCCA Hybrid Main Memory Systems Taxonomy), November 2014.
116. J. Lidman, S.A. McKee, D. Quinlan, C. Liao, "An Automated Performance-Aware Approach to Reliability Transformations", Workshop on Resiliency in High Performance Computing with Clouds, Grids, and Clusters (Resilience), August 2014.
117. D. Knyaginin, S.A. McKee, G.N. Gaydadjiev, "A Hybrid Main Memory Systems Taxonomy", Memory Architecture and Organization Workshop (MeAOW), October 2012.
118. J. Lidman, D. Quinlan., C. Liao, S.A. McKee, "ROSE::FTTransform — A Source-to-Source Transformation Framework for ExaScale Fault-Tolerance Research", Workshop on Fault Tolerance for HPC at Extreme Scale (FTXS), June 2012.
119. G. Goumas, S.A. McKee, M Själander, T.R. Gross, S. Karlsson, C.W. Probst, L. Zhang, "Adapt or Become Extinct!: the Case for a Unified Framework for Deployment-Time Optimization", Workshop on Adaptive Self-Tuning Computing Systems for the Exaflop Era (EXADAPT), June 2011, pp. 46-51.
120. M. Andersson, L. Svensson, M. Själander, S.A. McKee, E. Catovic, P. Ingelha, "Yield Optimization Using Redundant Cores", Swedish Workshop on Multi-Core Computing (MCC), pp. 30-33, October 2010.
121. M. Zahran, S.A. McKee, "Adaptive Block Placement Policy for Cache Hierarchies", Workshop on Statistical and Machine Learning Approaches to Architecture and Compilation (SMART), January 2009.
122. K. Singh, M. Bhadauria, S.A. McKee, "Real Time Power Estimation and Thread Scheduling via Performance Counters", Workshop on Design, Architecture, and Simulation of Chip-Multiprocessors (dasCMP), November 2008. ACM SigArch *Computer Architecture News*, 37(2):46-55, May 2009.
123. M. Zahran, S.A. McKee, "Enterprise-Like Cache Hierarchy Management in the Manycore Era", Workshop on Memory System Performance and Correctness (MSPC), March 2008.
124. P.A. Castillo, A.M. Mora, J.J. Merelo Guervós, J.L. Jiménez Laredo, M. Moretó, F.J. Cazorla, M. Valero, S.A. McKee, "Architecture Performance Prediction Using Evolutionary Artificial Neural Networks", EvoWorkshops, March 2008, pp. 175-183.
125. V.M. Weaver, S.A. McKee, "Are Cycle Accurate Simulations a Waste of Time?", Workshop on Duplicating, Deconstructing, and Debunking, June 2008.

126. M. Curtis-Maury, K. Singh, S.A. McKee, F. Blagojevic, D.S. Nikolopoulos, B.R. de Supinski, M. Schulz, "Identifying Energy-Efficient Concurrency Levels Using Machine Learning", International Green Workshop, September 2007, pp. 488-495.
127. E. Ipek, J.F. Martínez, B.R. de Supinski, S.A. McKee, M. Schulz, "Dynamic Program Phase Detection in Distributed Shared-Memory Multiprocessors", Workshop on the National Science Foundation Next Generation Software Program (NSF/NGS), April 2006, p. 280.
128. M. Schulz, B.S. White, S.A. McKee, H.S. Lee, "A Vision for Next-Generation System Monitoring", Workshop on Hardware Performance Monitor Design and Functionality, February 2005, pp. 65-74.
129. T. Suh, H.S. Lee, S.A. McKee, M. Schulz, "Evaluating System-Wide Monitoring Capsule Design Using Xilinx Virtex-II Pro FPGA", Workshop on Architecture Research using FPGA Platforms (WARFP), February 2005.
130. P.K. Szwed, D. Marques, R.M. Buels, S.A. McKee, M. Schulz, "SimSnap: Fast-Forwarding via Native Execution and Application-Level Checkpointing", Workshop on the Interaction between Compilers and Computer Architectures (INTERACT), February 2004.
131. Z. Fang, S.A. McKee, "MPEG4: Fallacies and Paradoxes", IEEE Workshop on Workload Characterization (WWC), November 2002, pp. 91-97.
132. T. Mohan, B.R. de Supinski, S.A. McKee, F. Mueller, A. Yoo, "Dynamic Detection of Streams in Memory References", Annual Symposium of the Los Alamos Computer Science Institute (LACSI), October 2001 (poster).
133. B.R. de Supinski, A. Yoo, F. Mueller, S.A. McKee, "Benchmarking SMP Memory Systems Performance", SCICOMP (IBM SP Scientific Computing User Group), October 2001.
134. F. Mueller, T. Mohan, B.R. de Supinski, S.A. McKee, A. Yoo, "Partial Data Traces: Efficient Generation and Representation", Workshop on Binary Translation (WBT), September 2001.
135. L. Zhang, S.A. McKee, J.B. Carter, W.C. Hsieh, "Prefetching within the Impulse Adaptable Memory Controller: Initial Results", Workshop on Solving the Memory Wall Problem, June 2000.
136. S.A. McKee, "Compiling for Efficient Memory Utilization", Workshop on the Interaction of Compilers and Computer Architecture (INTERACT), February 1996.

Refereed Tutorials

137. R. Figueiredo, co-PIs J.-K. Peir, J.A.B. Fortes, T. Li, P.O. Boykin, G.S. Tyson, L.K. John, D. Kaeli, D. Lilja, G. Memik, S.A. McKee, "Archer: Zero-Configuration Virtual Appliances for Architecture Simulation", in conjunction with IEEE International Symposium on Workload Characterization (IISWC), October 2009.
138. D. Brooks, B.R. de Supinski, B.C. Lee, S.A. McKee, M. Schulz, K. Singh, "Methods of Learning and Inference for Large Design and Parameter Spaces" in conjunction with ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2008.
139. S.A. McKee, K.Singh, D. Brooks, B.C. Lee, B.R. de Supinski, M. Schulz, "Inference and Learning for Large Scale Micro-Architectural Analysis", in conjunction with the ACM/IEEE International Symposium on Computer Architecture (ISCA), June 2007.

Newsletters

140. Wm.A. Wulf, S.A. McKee, "Hitting the Memory Wall: Implications of the Obvious", ACM SigArch *Computer Architecture News*, 23(1):20-24, March 1995 (cited 1200 times).

Software Artifacts

Adapteva Epiphany Simulator, O. Jeppsson, S.A. McKee (used in 114 and 115), soon to be part of the Adapteva Epiphany Chip SDK

LTE Uplink PHY Model, M. Själander, S.A. McKee, P. Brauer, D. Engdal (used in 40 and 43), an open-source, parameterizable benchmark to model workloads in an LTE base station (in collaboration with Ericsson AB, http://sourceforge.net/projects/lte-benchmark)

Fusion Predictive Modeling Tools, K. Singh, S.A. McKee (used in articles 10, 11, 50, 56, and 75) documentation: Cornell ECE technical report CSL-TR-2007-1049.pdf

Basic Block Vector Tools, V.M. Weaver, S.A. McKee (used in article 68) available from http://web.eece.maine.edu/~vweaver/projects/bbv_research/, merged into Valgrind

SimSnap (used in article 130), V.M. Weaver, P.K. Szwed, M. Schulz, S.A. McKee

Selected Research Projects

Creating a Representative Android Benchmark Suite 2015-present

P.I.s: G.S. Tyson (Florida State), S.A. McKee

There is currently no established benchmark suite for evaluating Android systems and the mobile devices on which they run. We are assembling a set of full, open-source applications that exercise the Android software architecture and that can be used to characterize and optimize architectural behavior. The suite spans a range of application categories and includes Java programs that run directly on the Android Operating System and C/C++ codes that rely on the Android Native Development Kit (NDK). The applications are suitable to run on native hardware, within the gem5 simulator, and within the Android Emulator. Mentoring FSU Ph.D. student Zachary Yannes and Chalmers M.S. student Mazdak Sanati.

Redesigning Data Center Servers 2013-present

PI: L. Zhang (Institute for Computing Technology, Chinese Academy of Sciences)

Collaborators: S.A. McKee, M. Huang (Univ. of Rochester)

The broader ICT project seeks to improve both performance and energy by redesigning data centers at all levels (from topologies and protocols to servers and memory systems). Collaborating on projects ranging from characterizing big data application behavior (to inform processor/system design); benchmark suite composition; software optimization; optimizing DRAM refresh power; and enabling inexpensive, flexible extended Buffer-on-Board memory systems; to developing hardware and software support for flexible resource sharing across server nodes. Supported by Chinese Academy of Sciences Presidential International Fellowship Initiative Visiting Scientist Award.

Exploiting Instruction Semantics to Save Power in the Microarchitecture 2011-present

PI: D. Whalley (Florida State)

Collaborators: P. Larsson-Edefors (Chalmers), S.A. McKee, M. Själander (Uppsala)

Techniques that rely on speculation to tolerate latency waste energy by guessing information that may already be deducible from the microarchitectural state and the instructions themselves. Investigating the addition of small, specialized cache-like structures next to the processor to avoid unnecessary tag checking, branch prediction, and L1 cache and TLB accesses. In many cases, these structures improve application performance, in addition to saving power.

Balancing Power and Performance 2008-2016

PI: S.A. McKee

Diminishing performance returns and increasing power consumption make power-aware resource management increasingly important in platforms ranging from supercomputers to embedded systems. For multithreaded programs, adding a core may harm performance *and* increase power consumption. Investigating mechanisms by which software components such

as hypervisors and operating systems can provide estimates of application performance and power consumption. Using this information to invoke appropriate power-saving policies to improve system-wide reliability and performance (e.g., through task scheduling, clock-gating cores, or reconfiguration). Created an open-source LTE (Long Term Evolution) baseband uplink benchmark (created in collaboration with Ericsson AB) to investigate power-aware resource management for LTE base stations. Advised Cornell Ph.D. students Karan Singh and Major Bhadauria, Chalmers postdoc Magnus Själander, and Chalmers masters/Ph.D. student Bhavishya Goel. Supported by NSF Awards 0325536 and 0444413, EC 7th Framework Programme awards 249059 and 610456, and Ericsson AB.

Multi-Platform SimPoints to Enable More Thorough Design Studies 2007-2009
PI: S.A. McKee

Developed multi-platform tools to generate Simulation Points (SimPoints) for accurate sampled execution simulations. We leveraged the widely adopted UCSD SimPoint methodology to enable accurate partial-simulation experiments, speeding architectural design space studies. Examined three binary instrumentation tools for generating SPEC2000 and SPEC2006 SimPoints across nine implementations of the IA-32 architecture. Created our own plug-ins for two tools, Qemu and Valgrind, and compared results to Intel's PinPoints. Validated our approaches via hardware performance counters, and verified the UCSD finding that multiple SimPoints must be modeled to generate accurate results: we modeled up to 20 to achieve error rates below 5%. Advised Cornell MS/Ph.D. student Vince Weaver.

The Chameleon Shared Memory System 2006-2008
PI: S.A. McKee
Collaborators: J.E. Moreira, S. Chiras, X. Shen (IBM T.J. Watson Research)

Developed a thin architectural layer to support shared memory in a Cell Broadband Processor-based blade system. We have implemented lightweight, FPGA-based hardware support for shared memory, enabling any processor to access SDRAM on any other blade via a DDR-2 memory controller and optical interconnect. This enables a lighter weight solution than traditional SMPs, since blades can be added one at a time. Likewise, it enables a more easily programmable system than clusters relying on message passing communication protocols. We thus attempt to deliver the best of both worlds (SMPs and clusters) at low cost. Advised Cornell masters student Chris D. Dolen. Supported via multiple IBM graduate internships at the T.J. Watson Research Center and an IBM Faculty Award.

High Performance, Energy-Efficient Memory Systems 2005-2008
PI: S.A. McKee Collaborator: G.S.Tyson (Florida State)

Explored alternative cache organizations for lower-power memory hierarchies for embedded and multicore systems. We have developed a simple, scalable policy for implementing drowsiness (lowering voltage on most lines to save leakage power) and cache decay. Adding drowsiness and column associativity to region-based caches saves energy without sacrificing performance in embedded systems. Adding our scalable drowsiness mechanism also works well with traditional CPUs and traditional L1/L2 cache hierarchies. Our cache decay mechanism operates as a snoop filter in multicore systems, saving both dynamic and leakage power with minimal effect on performance. Advised Cornell M.S. student Major Bhadauria and co-advised Michigan Ph.D. student Michael Geiger.

Predictive Models for Understanding and Improving Computer Systems Behavior 2003-2010
PI: S.A. McKee
Collaborators: B.R. de Supinski, M. Schulz (LLNL), D. Brooks (Harvard)

Growing system complexity combined with increasing usability and reliability requirements render many traditional architectural modeling techniques obsolete. Platforms affected range from mobile devices to desktops, high-throughput commercial systems to the high-end com-

puting systems that constitute our nation's most powerful supercomputers. Computer designs and accompanying workloads have grown sufficiently complex that modeling them fully in detail is simply intractable. Developed predictive models via Machine Learning approaches and statistical regression. Applied these techniques to predicting application runtimes for large-scale parallel scientific codes with large parameter spaces and to architectural design space exploration. In the former, we predict run times with 93-95% accuracies. For the latter, by sampling 1-2% of a full design space, we can predict IPC with 98-99% accuracies, on average. Advised M.S. student E. Ipek. Advised M.S. student K. Singh. Supported under NSF Awards ST-HEC 0444413 and CCF 0702616 and by internships at LLNL.

Understanding and Exploiting Phase Behavior of Parallel Programs 2004-2006
PI: S.A. McKee Co-PI: J.F. Martínez (Cornell)
Collaborator: B.R. de Supinski (LLNL)

Explored methods to identify phases in parallel programs at runtime and to use this information along with phase prediction to drive hardware reconfiguration. Much prior work has focused on dynamic phase-based behavior in uniprocessor or Simultaneous Multithreaded (SMT) applications, but we were first to provide solutions for parallel applications. The project addressed NUMA shared-memory systems. Advised M.S. student E. Ipek. Supported under NSF CNS Award 0509406 and by an internship at LLNL.

Optimizing Applications Using High-Level Abstractions 2003-2008
PI: D. Quinlan (LLNL) Co-PI: S.A. McKee

Developed compiler analysis and transformations necessary to optimize adaptive mesh-based codes that use libraries of abstractions in C++. The use of high-level programming abstractions, such as matrices and mesh entities, is a key to achieving productivity in scientific applications. Unfortunately, such abstractions frequently obfuscate compiler analysis because of their pervasive use of pointers or because they are implemented in libraries for which source code is unavailable. This work exploited the semantics of abstractions, as employed in unstructured mesh codes, to overcome the limits of compiler analysis and to guide domain-specific optimizations. Advised Ph.D. student B. White. Supported by DOE Krell Institute HPCS Fellowship under award DE-FG02-97ER25308 and DOE LLNL subcontract B571234.

System-Wide Hardware/Software Monitoring and Adaptation 2003-2008
PI: S.A. McKee Co-PI: H.S. Lee (Georgia Tech)

Investigated reconfigurable, continuous hardware monitors and the software to exploit them. As microarchitectural and system complexity grows, comprehending system behavior becomes increasingly difficult, often requiring gathering and sifting through voluminous event traces or coordinating results from multiple, non-localized sources. We addressed this complexity with a framework that deploys programmable elements throughout a system, locating hardware monitors at event sources. Monitors run and writeback results autonomously with respect to the CPU, avoiding large system overheads of interrupt-driven monitoring and removing the need to communicate irrelevant events to higher software levels. The framework is applicable to a broad range of monitoring goals, especially cluster communication and memory system performance: efficient memory access logging, runtime data collection for automatic optimization, memory access characterization through histograms, dynamic pattern recognition, heap access control, and network intrusion detection. Framework feasibility was supported by simulation results showing that, even with aggressive feedback, our monitors cause little system perturbation. Supported under NSF ITR/NGS Award 0325536.

Overcoming the Memory Wall for SMP Systems 2001-2002
PI: B.R. de Supinski (LLNL) Subcontract PI: S.A. McKee
Collaborators: A. Yoo, M. Schulz (LLNL), F. Mueller (LLNL/North Carolina State)
Led Utah/Cornell team developing better tools and metrics to evaluate memory behavior of parallel programs and design smarter SMP memory systems to exploit structured memory access patterns. Initial work created experimental infrastructure—in particular, a tool (METRIC) for dynamic partial address trace generation and analysis—and conducted initial studies of the memory system design space. Collaborated with SRC Computers, to investigate using reconfigurable processing elements to improve global memory performance. Advised (thesis) M.S. student T. Mohan and M.E. student I. Kumar. Supported by NSF CCR CSA award 0073532, DOE LLNL LDRD award 01-ERD-043 and an SBIR award with SRC Computers.

The Impulse Adaptable Memory System 1998-2002
PI: J.B. Carter Collaborators: S.A. McKee, W.C. Hsieh, A. Davis (Utah)
Co-led team building an adaptable main-memory controller that improves utilization of processor caches and system memory bus. By remapping unused physical addresses, the memory controller can access discontiguous data as if densely allocated, create superpages without copying, and aggressively prefetch within the memory controller without polluting caches. Studied effects of DRAM prefetching and scheduling, guided design of Parallel Vector Access Unit and development of analytic models of performance and remapping costs/benefits, and drove dissemination of research results. Co-advised (thesis) M.S. student B.K. Mathew. Mentored Ph.D. and masters students. Supported by DARPA Data Intensive Systems award.

A New Approach to Cache Analysis 1996-1998
PI: S.A. McKee Collaborator: Wm.A. Wulf (Virginia)
Developed an analysis methodology (viewing caches as filters) that provides the theory to support cache hierarchy design, along with mathematical tools and supporting software. Designed measures to graph locality in streams of memory requests, and developed tools to aid in the manipulation and interpretation of this data. Co-advised Virginia Ph.D. student D.A.B. Weikle. Supported by NSF POWRE Award 9806043 and NSF CCR CSA award 0073532.

The Stream Memory Controller (SMC) and the Weird Machine (WM) 1990-1996
PI: Wm.A. Wulf
Designed/developed hardware support (the SMC) for dynamic access ordering and memory access scheduling to increase memory hierarchy efficiency for streamed computations. Managed joint CS/EE SMC research group from 1995-96; managed CS side of project from 1994-96. Collaborated on design of operating system and architectural support for security for the WM machine. Maintained and augmented WM compiler/simulator. Supervised masters students. Led patent effort (awarded November 2000). Supported by NSF MIP award 9307626.

The Plan 9 Operating System 1988
Mentor: R. Pike
Added support for debugging to the Plan 9 operating system kernel, and then implemented an instruction-level debugger employing these kernel facilities.

Research Advising

Current Students

1. Ola Jeppsson, masters thesis student, Chalmers University of Technology.
2. Viktor Ahlin, masters thesis student, Chalmers University of Technology.
3. David Alm, masters thesis student, Chalmers University of Technology.
4. Mazdak Sanati, masters thesis student, Chalmers University of Technology.

Former Staff

1. Magnus Själander, Ph.D., Chalmers University of Technology. Postdoctoral Research Associate, 2010-present, Chalmers University of Technology. projects: Power-Aware Resource Management; Embedded Reconfigurable Architectures (1st position: Research Assistant Professor, Florida State University Department of Computer Science).
2. Daniel J. Marques, Ph.D., Cornell University. Postdoctoral Research Associate, Cornell University, March-August 2006. project: Automatic Application-Level Checkpointing for High Performance Computing Solutions (1st position: CTO at Ballista Securities, LLC).
3. Martin Schulz, Ph.D., Technische Universität-München. Postdoctoral Research Associate 2002-2004, Cornell University, projects: Hardware and Software for Efficient Memory Utilization in Uniprocessors and SMP Systems; System-Wide Monitoring and Adaptation; Middleware for Portable Parallel Programming (1st position: Computer Scientist at LLNL).
4. Gi-Ho Park, Ph.D. Yonsei University. Postdoctoral Research Associate 2000-2001, University of Utah, projects: Application-Specific Computer Architectures; The Impulse Adaptable Memory Controller (1st position: Samsung).

Graduated Students

Ph.D.

1. Bhavishya Goel, Ph.D. 2016, Chalmers University of Technology, dissertation: *Measurement, Modeling, and Characterization for Energy-Aware Computing*.
2. Peter K. Szwed, Ph.D. 2011, Cornell University, dissertation: *Transparent and Efficient Coherence for Aliased Physical Memory* (1st position: Senior Engineer at IBM Corp.).
3. Vincent M. Weaver, Ph.D. 2010, Cornell University, dissertation: *Using Dynamic Binary Instrumentation to Create Fast, Validated, Multi-Core Memory Simulation* (1st position: postdoctoral fellow, High Performance Computing, University of Tennessee; current position: Assistant Professor, Electrical and Computer Engineering, University of Maine).
4. Major B. Bhadauria, Ph.D. 2009, Cornell University, dissertation: *Thread Scheduling for Chip Multiprocessors*. *Canadian NSERC Graduate Fellow* (1st position: Senior Performance Hardware Engineer with EMC, Boston).
5. Karan Singh, Ph.D. 2009, Cornell University, dissertation: *Prediction Strategies for Power-Aware Computing on Multicore Processors* (1st position: Technical Advisor for Ropes and Gray L.L.P., Boston).
6. Brian S. White, Ph.D. 2008, Cornell University, dissertation: *A Semantics-Based Approach to Optimizing Unstructured Mesh Applications*. Dept. of Energy Krell Institute High-Performance Computer Science Fellow (1st position: postdoctoral fellow, Computational Bio-Physics, Cornell University; current position: Assistant Professor, Department of Medicine, Washington University St. Louis).
7. Dee A.B. Weikle, Ph.D. 2001, University of Virginia, dissertation: *A New Approach to Cache Analysis*. co-advised with Bill Wulf, 1997-2001 (1st position: Assistant Professor, Eastern Mennonite University; current position: Associate Professor, James Madison University).

Licentiate[1]

8. Jacob Lidman, Ph.Lic. 2015, Chalmers University of Technology, thesis: *Compiler Optimizations in the Presence of Uncertain Semantics.*
9. Bhavishya Goel, Ph.Lic. 2014, Chalmers University of Technology, thesis: *Topics in Power - Aware Computing.*

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1. This a Scandinavian degree awarded between masters and Ph.D.

Masters

10. Torbjörn Rasmusson, M.S. June 2016, Chalmers University of Technology, thesis: *A VHDLArchitecture for Auto Encrypting SD Cards* (with Alexander Davidsson).
11. Alexander Davidsson, M.S. June 2016, Chalmers University of Technology, thesis: *A VHDLArchitecture for Auto Encrypting SD Cards* (with Torbjörn Rasmusson).
12. Erik Alveflo, M.S. June 2015, Chalmers University of Technology, thesis: *Adaptive Core Assignment for Adapteva Epiphany.*
13. Erik Bergström, M.S. June 2015, Chalmers University of Technology, thesis: *A Distributed, Parallel and Fault Tolerant BGP Routing Daemon.* (with M. Millnert).
14. Martin Millnert, M.S. June 2015, Chalmers University of Technology, thesis: *A Distributed, Parallel and Fault Tolerant BGP Routing Daemon.* (with E. Bergström).
15. Dan Larsden, M.S. June 2015, Chalmers University of Technology, thesis: *Exploring the Generic Timer Module's Feasibility for Truck Powertrain Control.* (with J. Hemlin).
16. Jonas Hemlin, M.S. June 2015, Chalmers University of Technology, thesis: *Exploring the Generic Timer Module's Feasibility for Truck Powertrain Control.* (with D. Larsden).
17. Can Peskersoy, M.S. February 2013, Chalmers University of Technology (industrial masters, QLogic), thesis: *Extending Web Applications to Mobile Platforms*. (with M. Tanintara-Art).
18. Mary Maleekanya Tanintara-art, M.S. February 2013, Chalmers University of Technology (industrial masters, QLogic), thesis: *Extending Web Applications to Mobile Platforms*. (with C. Peskersoy).
19. Christian Lidberg, M.S. June 2012, Chalmers University of Technology (industrial masters, SAAB), thesis: *Optimization of FFB (Fast Factorized Backprojection) Execution Performance*. (with J. Olin).
20. Johan Olin, M.S. June 2012, Chalmers University of Technology (industrial masters, SAAB), thesis: *Optimization of FFB (Fast Factorized Backprojection) Execution Performance*. (coauthored with C. Lidberg).
21. Jacob Lidman, M.S. 2012, Chalmers University of Technology, thesis: *Increasing Parallelizing Compiler Efficiency Using Commutative Functions.*
22. Bhavishya Goel, M.S. 2011, Chalmers University of Technology, thesis: *Per-core Power Estimation and Power Aware Scheduling Strategies for CMPs.*
23. Anders Widén, M.S. 2010, Chalmers University of Technology, thesis: *Diabetic Care on Android Smartphones*.
24. Catherine Trammell, M.S. 2009, Cornell UniverEnergy-performance tradeoffs in processor architecture and circuit design: a marginal cost analysissity, thesis: *Exploring the Microarchitectural Behavior of an Industrial Processor in the Presence of Transient Faults*.
25. Christopher D. Dolen, M.S. 2007, Cornell University, thesis: *The Chameleon Shared Memory System*.
26. I-Chun Li, M.E. 2006, Cornell University, project: Converting a Cache Performance Analysis Tool to Use Valgrind for Application Trace Generation.
27. Engin Ipek, B.S. 2003, M.S. 2005, Cornell University, thesis: *Efficiently Exploring Architectural Design Spaces via Predictive Modeling*.
28. Amy Henning, M.E. 2005, Cornell University, research project: BlueGene/L: Improving Application Memory Performance on a Massively Parallel Machine. *Lawrence Livermore National Lab Fellow.*
29. Yong Hu, M.S. 2004, Cornell University, thesis: *Andromeda: a VIA-Based Software DSM System with Multithreading and Page Prefetching*.
30. Philip Sieh, M.E. 2004, Cornell University, project: Personal Inertial Navigation System.
31. Abhijeet Dhanapune, M.E. 2004, Cornell University, project: Performance Evaluation of Routing Protocols and Methods of Energy Conservation in MANETs.

32. Robert M. Buels, M.E. 2004, Cornell University, project: A Computer Vision System for Tracking Multiple Identical Zebrafish.
33. Venkata Tumati, M.E. 2004, Cornell University, project: MPEG4 Performance Analysis.
34. Biren Patel, M.E. 2004, Cornell University, project: Electronic Throttle Body.
35. Brad Kopek, M.E. 2003, Cornell University, project: The Common Messaging Layer over the Scalable Coherent Interface.
36. Jeremiah G. Ronquillo, M.E. 2003, Cornell University, project: Graphical User Interface for the emulegOS Capture the Flag Simulator.
37. Peter Wang, M.E. 2003, Cornell University, project: RF Communications Augmentation of the Lego Mindstorm RCX.
38. Tushar Mohan, M.S. 2003, University of Utah, thesis: *Detecting and Exploiting Memory Reference Regularity.*
39. Indrajeet Kumar, M.E. 2002, University of Utah, project: Balancing Memory Activity and Computation in Reconfigurable Co-Processors.
40. Binu K. Mathew, M.S. 2000, University of Utah, thesis: *Design of a Parallel Vector Access Unit*. co-advised with Al Davis (Ph.D. 2004 University of Utah.).
41. Chengqiang Zhang, M.E. 2000, University of Utah, project: Hardware-Only Stream Prefetching and Dynamic Access Ordering (Ph.D. 2008 University of Illinois Urbana-Champaign).
42. Hua Wang, M.E. 2001, University of Utah, project: Tools for Cache Analysis.

Bachelors Research Students

43. Ruke Ufomata, Cornell University, project: Advanced C Programming — Porting and Optimizing an Algorithm to Solve the Resource-Constrained Project Scheduling Problem, summer 2006-spring 2007. *Cornell Engineering Learning Initiatives (ELI) Fellow,* 2006-2007. *Cornell Presidential Research Scholar* 2007-2009.
44. William Baughman, Cornell University, project: Developing an Eclipse Open Source-Based GUI for the Jgraph Postscript Graphing Language, summer 2007-2008 (B.S. 2009).
45. Cathy Chen, Cornell University, project: Studying Custom Memory Hierarchy Design for Chip Multiprocessor Based Personal Electronics, *ELI Fellow* summer 2007-2008 (B.S. 2009).
46. Alexis A. Collins, Cornell University, project: Studying Custom Memory Hierarchy Design for Chip Multiprocessor Based Personal Electronics, summers 2007-2008 (B.S. 2009). *Cornell ELI Fellow.*
47. Chris Fromann, Cornell University, project: Learning the Ropes of Computer Systems Research, summer 2007-2008 (B.S. 2009).
48. Richard X. Yu, Cornell University, project: Learning the Ropes of Computer Systems Research, summer 2007-2008 (B.S. 2008). *Cornell Undergraduate Research Grant Fellow.*
49. Jessica Loeb, Cornell University, project: Studying Custom Memory Hierarchy Design for Chip Multiprocessor Based Personal Electronics, summer 2007-2008 (B.S. 2009).
50. Emmanuel Denloye, Cornell University, project: Studying Custom Memory Hierarchy Design for Chip Multiprocessor Based Personal Electronics, summer 2007-2008 (B.S. 2009).
51. D. Elias Bermudez, Cornell University, project: Pervasive System Monitoring, and Next-Generation Memory System Design, 2007-2008 (B.S. 2008). *Cornell ELI Fellow.*
52. David J. Drew, Cornell University, project: Compiling for C++ and Benchmark Suite Composition, summer 2006; High Performance, Energy Efficient Memory Hierarchies, 2007-2008 (B.S. 2008).
53. Siu Yu Cherie Kwan, Cornell University, project: Statistical Modeling of Architectural Parameter Correlations, 2006-2007 (B.S. 2008). *Cornell ELI Fellow.*
54. Christopher D. Leary, Cornell University, spring 2007, fall 2007-2008, projects: Building a Python-Based Graphical Interface for the Jgraph Graph Description Language; Hardware Support for Detecting Software Memory Access Bugs (B.S. 2008).

55. Huang Yu Ku, Cornell University, project: Statistical Modeling of Application Behavior for Architectural Design Space Exploration, summer 2006 (B.S. 2009).
56. Daniel Fitzgerald, Cornell University, project: Effective Communication and Dissemination of Research Results, summer 2006 (B.S. 2007).
57. Daniel Lee, Cornell University, project: Analyzing Dynamic Caching Efficiency on Modern Systems, summer 2005 (B.S. 2007). *Cornell University ELI student.*
58. James Juwon Lee, Cornell University, project: Compiling for C++ and Benchmark Suite Composition, summer 2006 (B.S. 2007). *Cornell University ELI student.*
59. Udit Agrawal, Cornell University, project areas: Debugging and Testing an RF Interface for LEGO Mindstorm Robots, 2003-2004; Faster Architectural Simulation Fast-Forwarding, 2005 (B.S. 2006). *Cornell Learning Initiatives for Future Engineers (LIFE) Fellow.*
60. Pamela Chuang, Cornell University, project areas: A User Interface for Configuring Reconfigurable Monitors; Faster Architectural Simulation Fast-Forwarding; (B.S. 2006). *Cornell ELI Fellowship/NSF REU student.*
61. Mark A. Berger, Cornell University, project areas: Exploring Hardware Assists for Exploiting Data Locality; Faster Architectural Simulation Fast-Forwarding, 2004-2005 (B.S. 2006, M.E. 2007). *NSF REU student.*
62. Pete J. Poulos, University of Utah, project: Simulation Tools to Model Adaptable Memory Controllers in SMP Systems, 2001 (B.S. 2005).
63. David B. Hodgdon, Cornell University, project areas: Distributed Shared Memory Clusters, and Porting the DynInst Toolset to the Macintosh OS-X (B.S. 2004).
64. Michael S. King, University of Utah, project: Simulation Tools to Model Adaptable Memory Controllers in SMP Systems, summer 2001 (B.S. 2002).
65. Laura Grit, CRA Distributed Mentor Project Intern (now Distributed Research Experiences for Undergraduates) intern, summer 2000 (Ph.D. 2007 Duke University).
66. Larissa Amy, CRA Distributed Mentor Project Intern (now Distributed Research Experiences for Undergraduates) intern, summer 1999 (M.S. 2006 University of Virginia).
67. Gergana Markova, CRA Distributed Mentor Project Intern (now Distributed Research Experiences for Undergraduates) intern, summer 1999 (M.S. 2003 Purdue University).

Pedagogical Training

Chalmers University of Technology/Gothenburg University, Gothenburg, SE

CIU930 Supervision of Research, 2014
Handledarforum (Supervisor Forum), 2013
GFOK025 Research Ethics and Sustainability, 2013

Olin College, Needham, MA

Meeting the Needs of the 21st Century: Designing for Student Engagement, June 2011
http://i2e2.olin.edu/summer/about.html

This highly participatory, week-long program helped participants develop designs and action plans for curricular changes at their institutions to meet future challenges: today's students will spend most of their working lives addressing problems that we have not yet imagined.

Cornell University, Ithaca, NY

Effective Teaching Workshop, R. Brent and R. Felder, January 2008
http://www4.ncsu.edu/unity/lockers/users/f/felder/public/Workshops.html

Workshop addressed how students learn, how teachers teach, and what often goes wrong in the process. Included course planning and how to be a be a better lecturer by actively involving students. Discussed inductive teaching methods, fair test creation, and common student-related problems and how to address them.

Cornell Information Technology Innovation in Teaching Project, 2003-2004

Designed (from scratch) masters-level course to instill confidence and communication, teamwork, and problem solving skills appropriate for careers in industry. The technical content of the course, "Engineering in the Real World", focused on the hardware/software interface by requiring the students to augment and program Lego Mindstorm robots to compete in a "Capture the Flag". Executing the course involved using multiple tools for content creation as well as assessment and reflection (including student self-assessment). See Cornell ECE595, below.

University of Virginia, Charlottesville, VA

Teaching Portfolio Workshop, October 1995

Workshop on developing portfolios (P. Seldin, "The Teaching Portfolio", 1991) that document teaching by including documents/artifacts along with analysis and commentary. Portfolios are intended for analytical self-reflection, documenting effectiveness and expertise, and strengthening research-teaching connections.

Teaching

Chalmers University of Technology, Gothenburg, SE

Instructor, DAT276/277, "Energy Aware Computing",
1 doctoral student, 16 masters students, spring 2016
1 doctoral student, 17 masters students, spring 2015

Supervisor/Mentor, DAT147, "Technical Writing"
3 masters students, fall 2016
6 masters students, fall 2015
4 masters students, fall 2014

Instructor, EDA281/EDA282, "Parallel Computer Organization and Design"
14 masters students, fall 2015
25 masters students, fall 2014
12 masters students, fall 2013
9 masters students, winter 2013
18 masters students, winter 2011
3 doctoral students, 20 masters students, winter 2010
1 doctoral student, 10 masters students, winter 2009

Institute for Computing Technology, Chinese Academy of Sciences, Beijing, CN

Instructor, "Technical Writing Bootcamp Workshop"
15 Ph.D. students, November, 2013

Cornell University, Ithaca, NY

Instructor, ENGRD150, "Engineering Seminar" (an introduction to engineering for majors)
16 freshmen, fall 2007
18 freshman students, fall 2003

Instructor, ECE685, "Memory Technologies and Systems"
6 Ph.D. students, 5 undergraduates, fall 2007
10 graduate (doctoral and MEng) students, 2 undergraduates, fall 2006 (taught as ECE 699)
7 doctoral students, 2 MEng students, fall 2005 (taught as ECE 699)

Instructor, ECE/COMS314, "Computer Organization"
155 undergraduate students (one Physics graduate student), spring 2007
172 undergraduate students, spring 2006
138 undergraduate students (one graduate ORIE student), spring 2005
140 undergraduate students, spring 2004

Instructor, ECE595, "Engineering in the Real World"
18 M.E. students, spring 2003
28 M.E. students, fall 2003
This pilot course strove to instill confidence and communication, teamwork, and problem solving skills appropriate for careers in industry. The vehicle for learning and practicing these skills was studying the hardware/software interface, where the hardware was a LEGO Mindstorm robot with a Hitachi H8 series microprocessor, and the software was BrickOS and C application programs. Students designed and implemented a "Capture the Flag" game and made videotaped oral presentations, multiple written reports, and team web portfolios.

University of Utah, Salt Lake City, UT

Instructor, CS5460, "Operating Systems"
70 undergraduate students, 10 graduate students, fall 2000
Co-Instructor, CS6935, "Computer Systems Seminar"
20 graduate students/staff, spring 1999
12 graduate students/staff, spring 1998

Oregon Graduate Institute, Portland, OR

Instructor, CSE585, "Advanced Memory Systems Architecture"
10 graduate students, fall 1997
Instructor, CSE522, "Advanced Computer Architecture"
12 graduate students, spring 1997

Reed College, Portland, OR

Co-Instructor, MATH442, "The Computer Science of Video Games"
12 undergraduate students, spring 1998
Dylan McNamee (then Asst. Prof. in CSE Dept. at OGI) and I created this broad, capstone course to teach Reed undergraduates fundamentals of Computer Science.

University of Virginia, Charlottesville, VA

Instructor, CS216, "Program and Data Representation"
12 undergraduate students, summer 1995
Teaching Assistant, CS360, "Computer Organization"
40 undergraduate students, fall 1990

Invited Talks

1. "Viewing the Computer As a Software Defined Network: Programmable Architectures for Resourcing-on-Demand", Chalmers University of Technology, Gothenburg, SE, May 2016 (innaugural lecture for promotion to full professor).
2. "A Flexible Approach to DRAM Refresh Management", Pacific Northwest National Laboratory, Richland, WA, US, June 2015.
3. "Memory System Innovations to Enable More Efficient Data Centers", Barcelona Supercomputer Center, ES, February 2015
4. "Memory System Innovations to Enable More Efficient Data Centers", Imperial College London, UK, December 2014.
5. "Techniques to Measure, Model, and Manage Power", Uppsala University, Uppsala, SE, December 2012.
6. "Tutorial on Per-Core Power Estimation for CMPs", HiPEAC Computing Systems Week, Barcelona, ES, October 2010.

7. “Comparing Scalability Prediction Strategies on an SMP of CMPs”, Uppsala University, Uppsala, SE, September 2010.
8. “Portable, Scalable, per-Core Power Estimation for Intelligent Resource Management”, Universitat Politècnica de Catalunya, Barcelona, ES, December 2009; IBM Austin Research Lab, Austin, TX, US, October 2009.
9. “Building Smarter Memory Systems from the Ground Up”, Chalmers University of Technology, Gothenburg, SE, June 2008.
10. “Using Dynamic Binary Instrumentation to Generate Multiplatform Simulation Points”, University of Wisconsin, Madison, WI, US, September 2007.
11. “Constructing Application Performance Models Using Neural Networks”, Schloss Dagstuhl International Conference and Research Center for Computer Science, Seminar 07341, Code Instrumentation and Modeling for Parallel Performance Analysis, August 2007.
12. “Architectural Design Space Exploration via Predictive Modeling”, University of California at Irvine, Irvine, CA, US, January 2007.
13. “Managing Complexity: Applying Predictive Modeling to Problems in Computer Engineering”, Cornell University, NY, US, January 2006 (Electrical and Computer Engineering Faculty Retreat).
14. “Architectural Design Space Exploration via Predictive Modeling”, University of Illinois at Urbana-Champaign, December 2006; University of Virginia, Charlottesville, VA, US, November 2006
15. ___, University of Michigan, Ann Arbor, MI, US, November 2006.
16. ___, Massachusetts Institute of Technology, Cambridge, MA, US, November 2006.
17. ___, Sun Microsystems, Santa Clara, CA, US, October 2006.
18. ___, Stanford University, Stanford, CA, US, October 2006.
19. ___, University of Rochester, Rochester, NY, US, September 2006.
20. “Memory System Optimizations for Performance and Low Power in Multicore-Based High-End Systems”, Computing Technologies Institute, Chinese Academy of Sciences, Beijing, CN, June 2006.
21. “Architectural Design Space Exploration via Predictive Modeling”, Computing Technologies Institute, Chinese Academy of Sciences, Beijing, CN, June 2006.
22. ___, National Institute for Research in Computer Science and Control (INRIA), Research Center, Rocquencourt, FR, May 2006.
23. “Dynamic Program Phase Detection in Distributed Shared-Memory Multiprocessors”, Rhodes, GR, April 2006 (invited workshop presentation).
24. “Architectural Design Space Exploration via Predictive Modeling”, IBM TJ Watson Research Center, Yorktown Heights, NY, US, February 2006.
25. ___, Cornell University, Ithaca, NY, US, February 2006.
26. “The Importance of ASC Funding to Computer Science Research”, Santa Fe, NM, US, October 2005 (panel at Annual Los Alamos Computer Science Institute (LACSI) Symposium).
27. “Architectural Design Space Exploration via Predictive Modeling”, Princeton University, Princeton, NJ, US, November 2005.
28. “Owl: An FPGA Prototype for Next-Generation System Monitoring”, Ohio Supercomputer Center-Springfield Operations Status Meeting, Lawrence Livermore National Laboratory, Livermore, CA, US, July 2005.

29. “Putting the ‘Real’ Into ‘Real-World Engineering’: Introducing Electronic Student Portfolios to Assess Student Learning”, Cornell University, Ithaca, NY, US, October 2003.
30. “Perspectives on the Memory Wall Problem”, Glen Eden, OR, US, April 2003, Salishan Department of Energy High Speed Computing Conference (invited presentation).
31. “Smarter Memory Controllers: a Parallel Vector Access Memory System”, the Pennsylvania State University, State College, PA, US, October 2002.
32. ___, Cornell University, Ithaca, NY, US, April 2002.
33. ___, University of Pittsburgh, Pittsburgh, PA, US, April 2002.
34. ___, IBM T.J. Watson Research Center, Yorktown Heights, NY, US, April 2002.
35. ___, University of California at Davis, Davis, CA, US, March 2002.
36. ___, Lawrence Livermore National Lab, Livermore, CA, US, March 2002.
37. ___, Brown University, Providence, RI, US, February 2002.
38. “Impulse: Building a Smarter Memory Controller”, University of British Columbia, Vancouver, BC, CA, January 2002.
39. “Smarter Memory Controllers: Improving Memory System Performance from the Bottom Up”, Technische Universität-München, Munich, DE, June 2000.
40. ___, Universitat Politècnica de Catalunya, Barcelona, ES, January 2000.
41. ___, Lawrence Livermore National Laboratories, Livermore, CA, US, December 1999.
42. ___, University of Illinois at Urbana-Champaigne, Urbana, IL, US, September 1999.
43. “Graduate School: Why Go, What to Look for, What to Expect”, Purdue University, West Lafayette, IN, US, September 1999.
44. “Maximizing Effective Memory Bandwidth for Streaming Computations”, University of California at Santa Barbara, Santa Barbara, CA, US, November 2001.
45. ___, University of Rochester, Rochester, NY, US, December 2001.
46. ___, University of Rhode Island, Kingston, RI, US, February 2002.
47. ___, Vanderbilt University, Nashville, TN, US, spring 1998.
48. ___, University of British Columbia, Vancouver, BC, CA, spring 1996.
49. ___, University of California at Davis, Davis, CA, US, spring 1996.
50. ___, University of Minnesota, Minneapolis, NM, US, spring 1996.
51. ___, Oregon Graduate Institute, Hillsboro, OR, US, spring 1996.
52. ___, Harvey Mudd College, Claremont, CA, US, spring 1996.
53. ___, Intel Corp., Portland, OR, US, spring 1996.
54. “How Virtual Memory Really Works”, Reed College, Portland, OR, US, spring 1998.
55. ___, Harvey Mudd College, Claremont, CA, US, spring 1996.
56. “The Stream Memory Controller”, Harvey Mudd College, Claremont, CA, US, spring 1996.
57. ___, Intel Research Forum, Portland, OR, US, April 1996.
58. “Adding Debugging Support to the Plan 9 Operating System”, Princeton, NJ, US, fall 1988.

Professional Service

Secretary

International Federation for Information Processing (IFIP) Working Group 10.3, 2016-present.

Advisory Boards

IEEE Technical Committee on Computer Architecture, 2001-2006.
ACM SIGMICRO, 2005-2009.
International Federation for Information Processing (IFIP) Working Group 10.3, 2009-2016.

Editorial Board

Springer *International Journal on Parallel Processing (IJPP)*, 2005-present.

Guest Editor

J.E. Moreira, V. Salapura, S.A. McKee, *Springer International Journal of Parallel Programming (IJPP)*, 39(1), February 2011.
S.A. McKee, *Journal of Instruction Level Parallelism (JILP)*, vol. 10, June 2008.
S.A. McKee, *ACM Transactions on Emerging Technologies (JETC),* 3(2), July 2007.
S.A. McKee, *EC Transactions on High Performance Embedded Architectures and Compilers (Trans. HiPEAC)*, 2(1) 2007 (special section).
S.A. McKee, *Springer International Journal of Parallel Programming (IJPP)*, 35(3), June 2007.
S.A. McKee, M. Schulz, B. Childers, K. Inoue, ACM SIGArch *Computer Architecture News,* 30(3), June 2002 (HPCA'02 Work in Progress Session).
S.A. McKee, M. Schulz, B. Childers, *IEEE Technical Committee on Computer Architecture (TCCA) Newsletter*, October 2001 (PACT'01 Work in Progress Session).
S.A. McKee, *IEEE Technical Committee on Computer Architecture (TCCA) Newsletter*, spring 2000 (HPCA'00 Work in Progress Session).

Steering Committees

ACM International Conference on Computing Frontiers (CF), May 2005-present.
ACM International Conference on Supercomputing (ICS), June 2011-present.
IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT), October 2002-2004, September 2009-September 2011.

General Chair

ACM/IEEE/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT) (with M. Schulz, Lawrence Livermore National Laboratory), September 2009.

Sponsorship Chair

IEEE International Symposium on Performance Analysis of Software and Systems, April 2017.

Program Committee Chair

Euro-Par track on High Performance Architectures and Compilers, August 2014.
ACM International Conference on Computing Frontiers, (with D. Franklin, University of California Santa Barbara), May 2014.
Workshop on Infrastructure for Hardware/Software Co-Design (WISH) at Code Generation and Optimization (with N. Neelakantam, Intel), April 2012.
First International Workshop on Power Measurement and Profiling (PMP) at IEEE International Green Computing Conference (with W. Shi, Wayne State University), June 2011.
ACM International Conference on Supercomputing (ICS) (with B.R. de Supinski, Lawrence Livermore National Laboratory), June 2011.

Workshop on Infrastructure for Hardware/Software Co-Design (WISH) at ACM/IEEE International Conference on Code Generation and Optimization (with R. McGeer, Hewlett Packard), April 2011.
ACM International Conference on Computing Frontiers (CF), May 2006.
New Investigator Papers, ACM/IEEE Grace Murray Hopper Celebration of Women in Computing (GHC), October 2004.
IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT) (with E. Altman, IBM T.J. Watson Research), September 2002.

Program Committees

Workshop on Architectures and Systems for Big Data (ASBD), Chairs: J. Kim, X. Sui, June 2016.
IEEE/ACM International Symposium on Cluster, Cloud, and Grid Computing (CCGrid), Performance Modeling and Evaluation Track Chair: M. Schulz, May 2016.
ACM International Conference for High Performance Computing, Networking, and Storage (SC), Doctoral Showcase Committee, Chair: M.C. Smith, November 2015.
International Symposium on Memory Systems (MEMSYS), Chair: B.L. Jacob, October 2015.
IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT), Chair: M. Snir, October 2015.
ACM International Conference on High Performance Computing, Networking, Storage, and Analysis (SC), Doctoral Showcase Committee, Chairs: M.C. Smith, V. Kindratenko, November 2015.
ACM International Conference on Supercomputing (ICS), Chairs: F. Chong, V. Sarkar, June 2015.
ACM International Conference on Computing Frontiers (CF), Chairs: H. Franke, R. Hou, May 2015.
ACM International Conference on High Performance Computing, Networking, Storage, and Analysis (SC), Computer Architectures and Networks track, Track Chairs: K. Shaw, S. Reinhardt, November 2014.
IEEE International Symposium on Workload Characterization (IISWC), Chairs: L. Tang, L. Zhang, October 2014.
International Workshop on OpenMP (IWOMP), Chairs: B.R. De Supinski, L. DeRose, September 2014.
ACM SIGPLAN Workshop on Memory System Performance and Correctness (MSPC), Chairs: T. Harris, M. Kulkarni, June 2014.
Workshop on Multithreaded Architectures and Applications (MTAAP), Chair: L. DeRose, May 2013.
IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), Chair: T.M. Aamodt, April 2013.
IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT), Chairs: D. Lilja, L. DeRose, September 2012.
International European Conference on Parallel and Distributed Computing (Euro-Par), with A. Malony, Performance Prediction and Evaluation track, Track Chair: A. Malony, August 2012.
ACM/IEEE International Symposium on Code Generation and Optimization (CGO), Chairs: U. Srinivasan, S. Amarsinghe, March 2012.
IEEE/IFIP International Symposium on Computer Architecture and High Performance Computing Software (SBAC-PAD), Chair: L. DeRose, October 2012.
IEEE International Conference on Computer Design (ICCD), Chairs: A. Ramirez, S. Sair; October 2011.
Euromicro Conference on Digital System Design, Chair: P. Kitsos, August 2011.
IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT), Chairs: M. Gschwind, J. Knoop; September 2010.

IEEE International Conference on Computer Design (ICCD), Chairs: J. Bondi, B. Juurlink; October 2010.

IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), Chair: D. Brooks; March 2010.

5th Annual EC International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), Chairs: E. Duesterwald, P. Faraboschi; January 2010.

ACM International Conference on Supercomputing (ICS), Chairs: J. Moreira, V. Salapura; June 2009.

ACM/IEEE International Symposium on Computer Architecture (ISCA), Chair: W.W. Hwu; June 2008.

IEEE International Parallel and Distributed Processing Symposium (IPDPS), Chair: Y. Robert, Architecture Track Vice-Chair, D. Kaeli; April 2008.

ACM SIGPLAN Workshop on Memory Systems Performance and Correctness (MSPC), with ACM 13th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Chair: B.Chen; March 2008.

Workshop on Design, Architecture, and Simulation of Chip Multiprocessors (dasCMP), with IEEE/ACM 40th Symposium on Microarchitecture (MICRO), Chairs: N. Jouppi, R. Kumar, D. Tullsen; December 2007.

Workshop on Experimental Computer Science (ExpCS), with the ACM Federated Computer Research Conferences (FCRC), Chairs D. Feitelson, L. Rudolf; June 2007.

2nd Workshop on Modeling, Benchmarking, and Simulation (MoBS), with the ACM/IEEE International Symposium on Computer Architecture (ISCA), Chairs: L. Eeckhout, J.J. Yi; June 2007.

1st Workshop on Statistical and Machine Learning Applied to Architectures and Compilation (SMART), with EC International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), Chairs: J. Cavazos, G. Fursin; February 2007.

International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), Chairs: P. Stenström, D. Whalley; February 2007.

IEEE International Parallel and Distributed Processing Symposium (IPDPS), Chair: A. Rosenberg, Architecture Track Vice-Chair: A. Gottlieb; April 2006.

4th Workshop on Memory Performance Issues (WMPI'06), with IEEE Symposium on High Performance Computer Architecture (HPCA), Chairs: J.B. Carter, L. Zhang; February 2006.

1st Workshop on Introspective Architectures (WISA'06), with IEEE Symposium on High Performance Computer Architecture (HPCA), Chairs: H.S. Lee, T. Mudge, M. Prulovic; February 2006.

ACM Workshop on Memory Performance: Dealing with Applications, Systems, and Architecture (MEDEA), with IEEE/ACM International Conference on Parallel Architectures and Compilation Techniques (PACT), Chairs: S. Bartolini, R. Giorgi; September 2005.

IEEE International Conference on Computer Design (ICCD), Chairs: D. Brooks, M. Gschwind; October 2005.

ACM International Conference on Supercomputing (ICS), Chair: L. Rudolph; June 2005.

IEEE International Workshop on Interaction between Compilers and Architectures (INTERACT), with IEEE Symposium on High Performance Computer Architecture (HPCA), Chair: W.C. Hsu; February 2005.

IEEE International Symposium on High Performance Computer Architecture (HPCA), Chair: J. Duato; February 2004.

IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT), Chairs: M. Hall, V. Sarkar; September 2003.

IEEE International Symposium on Modeling, Analysis and Simulation of Computers and Telecommunication Systems (MASCOTS), Chair: D. Nicol; August 2001.

IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT), Chair: M.L. Soffa; October 2000.
IEEE International Conference on Parallel Processing (ICPP), Chair: D. Lilja; August 2000.
Workshop on Solving the Memory Wall Problem, with ACM/IEEE International Symposium on Computer Architecture (ISCA), Chairs H. Hadimioglu, D. Kaeli; June 2000.
IEEE International Symposium on High Performance Computer Architecture (HPCA), Chair: K. Li; January 2000.
IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT), Chairs: P. Evripidou, G. Silberman; October 1999.
IEEE International Conference on Computer Design (ICCD), Chair: L. John; October 1999.
IEEE/ACM International Workshop on Computer Architecture for Machine Perception (CAMP), Chair: C. Weems; October 1997.

Workshops Chair

ACM/IEEE International Symposium on Computer Architecture (ISCA), June 2008.
ACM/IEEE International Symposium on Computer Architecture (ISCA), June 2004.

Treasurer/Registration Chair

ACM International Conference on Computing Frontiers (CF), May 2005.

Publications Chair

ACM International Symposium on Microarchitecture (MICRO-38), November 2005.
IEEE International Symposium on High Performance Computer Architecture (HPCA), January 2001.
IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT), October 1999.

Publicity Chair

First International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), November 2005.
IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT), September 2001.

Sponsorship Chair

IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), April 2017.

Workshop/Session Organizer

CRA/CDC/NSF/Intel/IBM Computer Architecture Summer School Workshop (with I. Bahar, Brown University; M.J. Irwin, The Pennsylvania State University; R. Joseph, Northwestern University; M.R. Martonosi, Princeton University; L. Peh, Princeton University; K. Shaw, University of Richmond; part of NSF *Broadening Participation in Computing*), July 2006.
IEEE International Symposium on High Performance Computer Architecture (HPCA) Work In Progress Session, February 2002.
IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT) Work In Progress Session, September 2001.
ACM/IEEE Grace Murray Hopper Celebration of Women in Computing CRA DMP Mentoring Workshop, September 2000.
IEEE International Symposium on High Performance Computer Architecture (HPCA) Work In Progress Session, January 2000.

Scholarship Committees

ACM/IEEE Grace Murray Hopper Celebration of Women in Computing (GHC), September 2000.

Invited Conferences/Workshops/Seminars

DOE ModSim Workshop on Modeling and Simulation, Seattle, WA, August 2015, 2016.
Intel High-End Computing Roundtable, Salt Lake City, UT, November 2012.
DOE High Speed Computing Conference (Salishan), Glen Eden Beach, OR, April 2003, 2004, 2005, 2007, 2010.
Seminar 07341: Code Instrumentation and Modeling for Parallel Performance Analysis, Schloss Dagstuhl, DE, August 2007.
Los Alamos Computer Science Institute (LACSI), Santa Fe, NM, October 2005.
DOE High-End Computing Revitalization Task Force (HECRTF), Washington, DC, June 2003.
DOE Scientific Case for Large-Scale Simulation (SCaLeS), Arlington, VA, June 2003.
Intel High-End Computing Roundtable, Chantilly, VA, August 2003.

University Service

Chalmers University of Technology, Gothenburg, SE

Computer Science and Engineering
Counselor: IEEE Women in Engineering Student Branch Affinity Group (2015-)
Computer Engineering Web Presence Redesign Committee (2016-)
Licentiate Opponent: David Eklöv (Uppsala University, 2011), Andreas Sembrant (Uppsala University, 2012)
Member of Doctoral Committee: Faheem Ullah (ETH-Zurich, 2016), Ananya Muddukrishna (KTH, 2016), Ahmed Ali-Eldin (Umeå University, 2015), David Eklöv (Uppsala University, 2012), Anna Bosque (Universidad de Zaragoza, 2011), Marius Grannaes (Norwegian University of Technology and Science, 2010), Rubén Gonzalez (Universitat Politécnica de Catalunya, 2009)
Promotion/Hiring Review Board (Danish Technical University, 2010)
Distinguished Speaker Colloquium Series Organizer, 2010-2012
Member of Graduate Group (approving defense committee members), 2010-2013

Cornell University, Ithaca, NY

School of Electrical and Computer Engineering
Member of Special Committees: M. Watkins, B. Keller, S.J. Jackson, A. Browder (ECE, M.S. 2007), G. Bronevetsky, R. Fernandes (CS, Ph.D. 2006), M. Khalili (ECE, Ph.D. 2005), J.R. Teifel (ECE, Ph.D. 2004)
Undergraduate Advising, 2003-2008
Electrical and Computer Engineering Computing Committee, 2003-2008
Computer Science Field Qualifying Exam Committee, 2003
Computing Research Association Representative, 2002-2008

University of Utah, Salt Lake City, UT

School of Computing
Member of Doctoral Committees: Z. Fang (Ph.D. 2006), B. Chandramouli (M.S. 2002), V.S. Pingali (M.S. 2002), L. Schaelicke (Ph.D. 2001), L. Zhang (Ph.D. 2003)
Graduate Studies Committee, 2001-2002
Graduate Recruiting, 2001-2002
Ph.D. Qualifying Exam Committee, fall 2000
Computer Policy Committee, 1999-2000

Graduate Recruiting Committee, 1998-1999 (co-organized Graduate Recruiting Visit)
Faculty Recruiting, Systems Subcommittee, 1998-1999
ACM Student Programming Competition
Utah Assistant Coach, November 1999
Regional Competition Judge, November 1999
Intermountain Junior Science and Humanities Competition Judge, 1999

University of Virginia, Charlottesville, VA

Computer Science Department
Member of Graduate Committees:
D.A.B. Weikle (CS, Ph.D. 2001), S. Hong (EE, M.S. 1999)
Undergraduate Curriculum Committee, 1993-1995
Library Committee, 1992-1995
Youth Summer Enrichment Program: Laboratory Instructor, 1994

Professional Society Memberships

Association for Computing Machinery (SIGARCH, SIGMICRO, SIGHPC), Senior Member
International Association for Electrical and Electronics Engineers Computer Society (TCCA, WIE), Senior Member
American Association of University Women (former)
American Association for the Advancement of Science (former)

Erdös Number 3 (via Gabriel Robins and Andrew Kahng)