# Master thesis - MCCX04

## Carbon nanotube TSV development towards all-carbon IC devices

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**Project description**

Moore's law has pushed the development of performance and profitability regarding integrated circuits (ICs) in an exponential fashion over the last couple of decades. With the scaling now reaching critical dimensions this development is starting to slow down. In order to continue improving ICs further the industry have suggested 3D packaging as one way forward. By stacking multiple dies on top of each other, the performance of IC devices can continue scaling without increasing the IC footprint. However, copper interconnects face acute resistivity issues when scaling down to cross sectional dimensions below 40 nm with severe performance and reliability impacts as a result. Instead, nanomaterials like graphene and carbon nanotubes have been proposed for use as new interconnect materials for VLSI due to their intrinsic material properties that allows them to scale further than copper.

In this project, bundles of carbon nanotubes coated with copper will be fabricated for use in through silicon VIA (TSV) applications aimed towards the development of all carbon IC devices. These carbon nanotube TSV structures will be optimized for their current carrying capability by tuning the bundle density, crystallinity and copper fill factor. The carbon nanotubes will be synthesized in the MC2 cleanroom by the means of photolithography, e-beam deposition and chemical vapor deposition. Various equipment will be utilized in order to evaluate the quality of the materials by the use of SEM, Raman, XPS and AFM to name a few.

Students with a background in chemistry, physics, nanotechnology or equivalent are preferred.

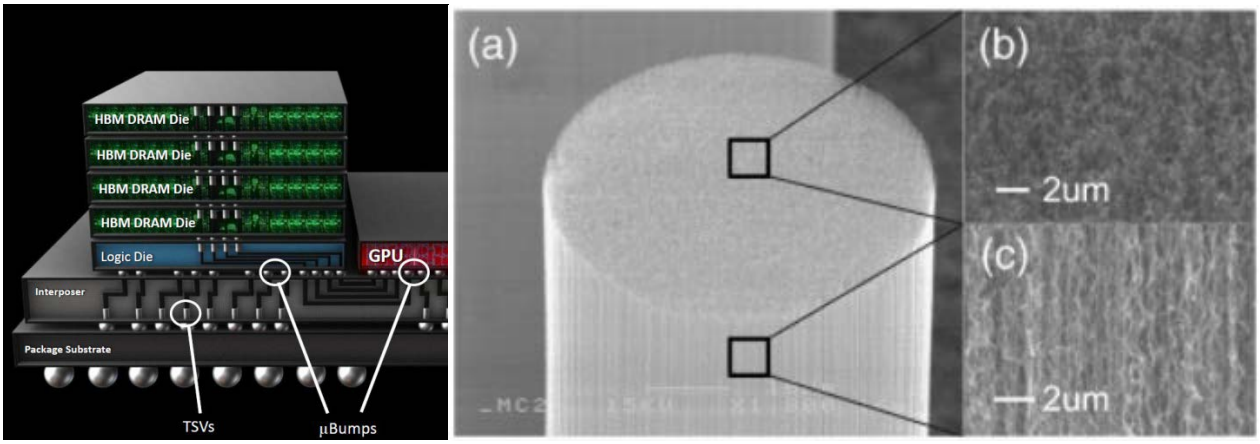


*Figure: Left – A schematic of TSV implementation in modern 3D stacked IC devices. Right – A carbon nanotube bundle grown using the CVD process.*